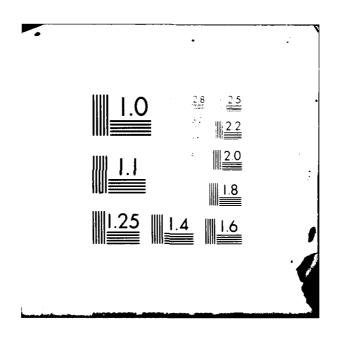
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POWER CONDITIONING SUBSYSTEM DESIGN



J. J. Moriarty, Et al

January 1982

Interim Report for Period 17 September 1979 - 30 November 1981

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O. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This interim report describes the results of the first two phases of a 3-phase program to provide designs of lightweight, low volume power conditioning subsystems in the range of 500 kilowatts (kW) to 30 megawatts (MW) as part of the Air Force exploratory development program in high power airborne electrical power supply technology. These designs are based on presently available component technology such as solid-state switching devices, newly developed thyratons and high energy density capacitors. Although these

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subsystems are to be operated in a burst mode, active cooling concepts have been utilized wherever they would result in an advantage in weight or volume.

Preliminary designs and approaches were determined for each of the subsystems in Phase I. In addition, those component parameters were identified which appeared to be critical in achieving minimum weights and volumes.

In Phase II detailed designs resulting in weight, volume, cooling requirements, and efficiencies have been determined for a selected group of operating points for each subsystem. The total number of operating points for all four subsystems is 296. The actual number of designs completed was less because of insurmountable limitations in SCRs for the inverter application.

FOREWORD

This interim report was submitted by Raytheon Company, Missile Systems Division, Bedford Laboratories, Bedford Massachusetts 01730 under Contract F33615-79-C-2079. The effort was sponsored by the Air Force Aero Propulsion Laboratory, Air Force Wright Aeronautical Laboratories, Air Force Systems Command, Wright Patterson AFB, Ohio 45433 under Project 3145-32-54. Capt. Fred Brockhurst was the Project Engineer at the beginning of the project. Capt. Jerry Clark is currently the Project Engineer. The time period covered by the report is September 17, 1979 through November 30, 1981.

The detailed designs were performed primarily by John Moriarty (Principal Investigator), Alvin Herling, John Kelleher and Donald Shute. Preliminary designs were prepared by Gordon Simcox, David Donovan ad Donald Bingley. Preliminary and detailed designs of unique magnetic components were performed by Paul Corbiere.

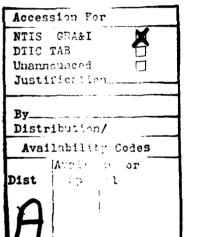




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1 INTRODUCTION

This interim report describes the results of the first two phases of a three-phase program to provide designs of lightweight, low volume power conditioning subsystems in the range of 500 kilowatts (kW) to 30 megawatts (MW) as part of the Air Force exploratory development program in high power airborne electrical power supply technology. These designs are based on presently available component technology such as solid state switching devices, newly developed thyratrons and high energy density capacitors.

Although these subsystems are to be operated in a burst mode, active cooling concepts have been utilized wherever they would result in an advantage in weight or volume. Burst duration, duty cycle and environmental requirements have been modified wherever possible to minimize weights and volumes.

Preliminary designs and approaches were determined for each of the subsystems in Phase I. In addition, those component parameters were identified which appeared to be critical in achieving minimum weights and volumes.

In Phase II detailed designs resulting in weight, volume, cooling requirements and efficiencies have been determined for a selected group of operating points for each subsystem. The total number of operating points for all four subsystems is 296. Since each point would result in a separate design for minimum weight and minimum volume, a total of 592 point designs have been undertaken. The actual number of designs completed was less because of insurmountable limitations in SCRs for the inverter application. It is understood that these point designs will be used by the Air Force to generate algorithms for computerized systems feasibility studies.

Improvements which can be projected in the critical device parameters will be compiled by the Air Force with the cooperation of device manufacturers. In Phase III, the detailed designs of Phase II will be modified where appropriate to show reductions in weight and volume that may be expected with the projected improvements in device parameters. A summary of the subsystem specification ranges is shown in Figure 1 in the form of a block diagram for a typical system which could be composed of the subsystems under study. Only those subsystems shown below the dashed line in the figure are considered in this study. Furthermore, interfacing components between subsystems have not

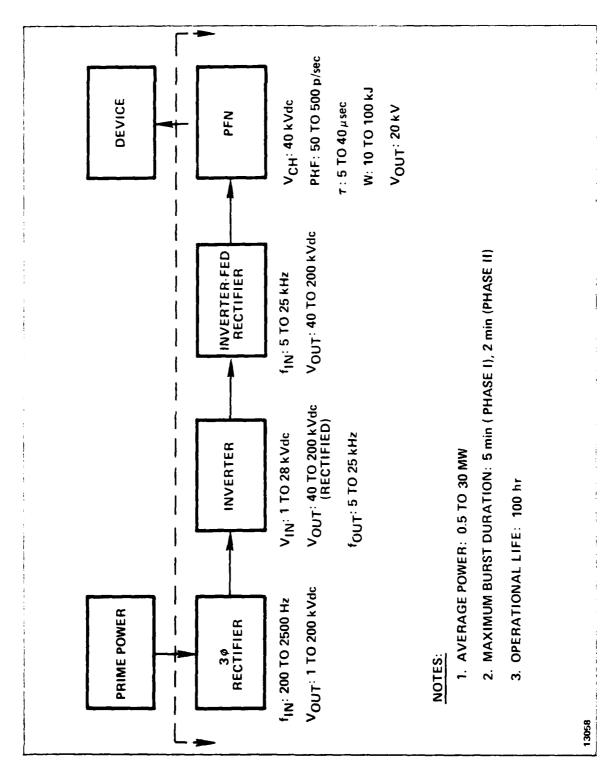


Figure 1 - General Subsystem Specifications

been included, since such components would vary considerably with overall system packaging and insulation approaches. It should be understood that many complete systems could be conceived which would not include all four subsystems shown in the block diagram.

The environmental and operational limitations used in Phase I are summarized below:

Ambient air and water temperature: 20°C

• Active cooling media: circulating air and water

• Altitude: sea level to 10,000 ft

Burst duration: 5 min.

Operating life: 100 hr

In an effort to reduce the subsystem size and weight, these restrictions were modified in Phase II as follows:

• Active cooling media: air, oil, water, Freon

Burst duration: 2 min.

A summary of the Phase I results is given in the next section, and the Phase II designs for each of the subsystems are described in the four subsequent sections.

2. PHASE I PRELIMINARY DESIGNS

The purpose of Phase I was to develop design concepts for the four subsystems and to test these concepts by preparing preliminary designs in both minimum weight and minimum volume configurations at six design points within the range of interest for each subsystem. In addition, this preliminary design effort was required to determine those device parameters which would have a critical effect on subsystem weight or volume.

The results of this effort were presented to Air Force and device manufacturer audiences on the 12th and 26th of February 1981. The following paragraphs briefly summarize the material that was presented.

2.1 Three-Phase Rectifiers

Designs of the three phase rectifiers were formulated at low and medium power levels because of component availability. A low, medium and high frequency design point was selected to examin. The power dissipation. The schematic in Figure 2 shows the components examined in this design.

The electrical design approach was based on 50 percent voltage derating and 30 percent current derating of the SCRs. In these designs, the current derating was actually greater than 30 percent because of limited component selections. Although the junction temperature was not used as a design parameter, it was not allowed to exceed 90 percent of the manufacturer's rating.

A maximum module voltage of 50 kV was chosen to limit to 55 the number of SCRs to be connected together in series. It was felt that other points in the 200 kV range could be attained by means of stacking the 50 kV modules. It was necessary to water-cool the SCRs and therefore to have sufficiently long, cool, dielectric tubing to provide higher voltage isolation through the water.

The results of the mechanical design are more readily categorized by cooling technique than by the reduction of weight or volume. As shown in Tables 1, 2, and 3, the air-cooled designs are generally lower in weight, whereas water-cooled designs are lower in volume.

Critical SCR parameters which were found to affect these designs include component packaging, reverse recovery, reverse breakdown and forward current ratings. Of these, component packaging had by far the greatest influence.

2.2 Inverter-Fed Rectifiers

The power and frequency range of the inverter-fed rectifier design points were based on the same rationale as was used to select the three-phase rectifier points. A maximum module voltage of 40 kV was chosen to limit to 125 the number of rectifiers to be connected in series. Modular stacking was assumed for point design voltages up to 200 kV. The components of a 40 kV module are shown within the dashed lines of the schematic in Figure 3.

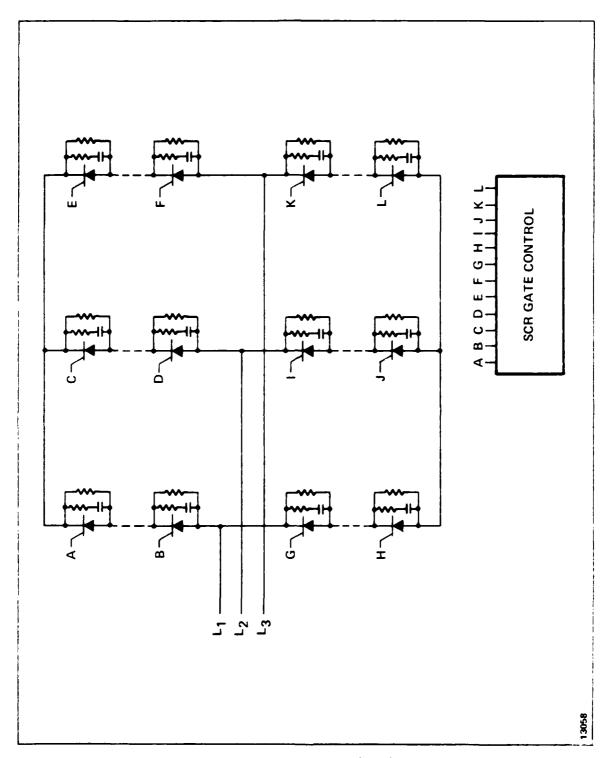


Figure 2 - Three Phase Rectifier (SCR) Schematic

TABLE 1
THREE-PHASE RECTIFIERS SUMMARY

POWER (MW) VOLTAGE (kV dc) FREQUENCY (Hz)	0.5 1.0 200	0.5 1.0 1200	0.5 1.0 2500	14 50 200	14 50 1200	14 50 2500
AIR-COOLED						
WEIGHT (1b) VOLUME (ft ³) DENSITY (1b ft ³)	37 0.52 71.2	180 3. 58.		1765 32 55.2		
WATER-COOLED						
DRY WEIGHT (1b) WET WEIGHT (1b)	23.7 24.5	94.8 98	3		868 903	
VOLUME (ft ³) DENSITY (lb/ft ³)	0.55	2.: 44.:			41.9 21.6	
PWR/VOL (kW/ft ³) PWR/WT (kW/lb)	909 20.4	228 5.1		334 15.5		
HEAT LOAD (kW) EFFICIENCY (%)	0.81 - 99.8	6.67 98.7	7.85 98.4	28.5 99.8	47.6 99.7	66.1 99.5
SCR TYPE (GE)	613L	C444M	C444M	613L		

TABLE 2
THREE-PHASE RECTIFIERS - AIR-COOLED PARAMETERS

Point Design #	1	2	3	4	5	6
POWER MW	0.5	0.5	0.5	14	14	14
VOLTAGE KVDC	1.0	1.0	1.0	50	50	50
FREQUENCY H2	200	1200	2500	200	1200	2500
WEIGHT DRY lb. WEIGHT WET lb. VOLUME ft ³ DENSITY lb/ft ³	37	180	180	1765	1765	1765
	-	-	-	-	-	-
	0.52	3.09	3.09	31.96	31.96	31.96
	71.2	58.3	58.3	55.23	55.23	55.23
TOTAL HEAT LOSS kW COOLING AIR 20°C AMB. CFM \$\Delta\$ P in-H20 \$\Delta\$ T C°	0.81	6.67	7.85	28.5	47.6	66.1
	85.5	950	950	9492	9492	9492
	≤0.5	2.0	2.0	≤0.4	≤0.4	≤0.4
	24.5	18.0	21.0	7.8	13.0	18.0

TABLE 3
THREE-PHASE RECTIFIERS - WATER-COOLED PARAMETERS

Point Design #	1	2	3	4	5	6
POWER MW	0.5	0.5	0.5	14	14	14
VOLTAGE kVDC	1.0	1.0	1.0	50	50	50
FREQUENCY Hz	200	1200	2500	200	1200	2500
WEIGHT DRY 1b. WEIGHT WET 1b. VOLUME ft ³ DENSITY 1b/ft ³	23.7	94.8	94.8	868	868	868
	24.5	98.0	98.0	903	903	903
	0.55	2.19	2.19	41.94	41.94	41.94
	44.55	44.75	44.75	21.53	21.53	21.53
TOTAL HEAT LOSS kW WATER COOLING 20°C AMB. GPM \$\Delta\$ P PSI \$\Delta\$ T C°	0.81	6.67	7.85	28.5	47.6	66.1
	1.0	1.0	1.0	12.0	12.0	12.0
	2.0	8.0	8.0	16.0	16.0	16.0
	3.0	25.0	29.5	9.0	15.0	20.9

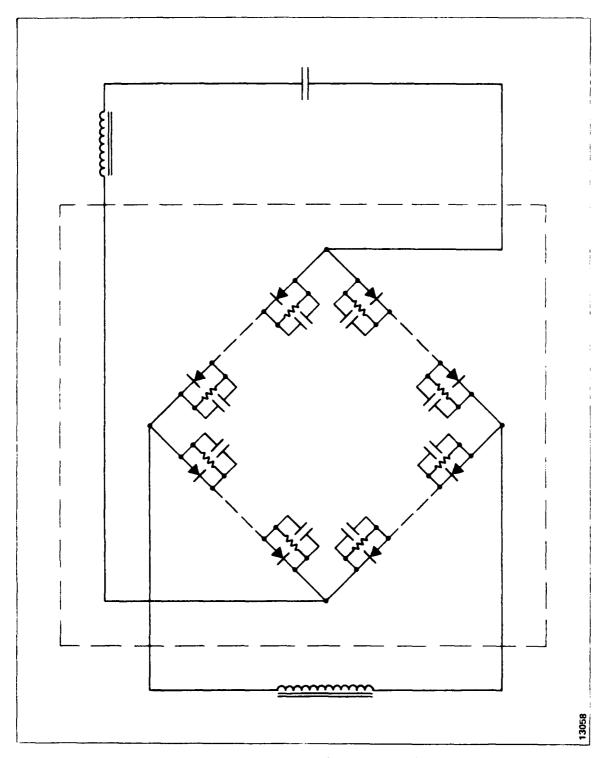


Figure 3 - Inverter Fed Rectifier (40 kV Module) Schematic

Water cooling was provided to the rectifiers by means of long, coiled, dielectric tubing to provide high voltage isolation in the water. Weight and volume of the preliminary designs were found to depend only on average power level. Distinct concepts and designs for minimum weight and minimum volume were not found. The results are summarized in Tables 4 and 5.

Critical diode parameters were found to be similar to those listed for SCRs in the three-phase rectifiers.

TABLE 4
INVERTER-FED RECTIFIERS SUMMARY

POWER (MW) VOLTAGE (kV dc) FREQUENCY (kHz)	0.5 40 5	0.5 40 15	0.5 40 25	7 80 5	7 80 15	7 80 25
DRY WEIGHT (1b) WET WEIGHT (1b) VOLUME (ft ³) DENSITY (1b/ft ³)		157 169 6.75 25			1374 1440 50 28.8	
PWR/VOL (kW/ft ³) PWR/WT (kW/lb)		74 3			140 4.9	
HEAT LOAD (kW) EFFICIENCY (%)	11.2 97.8	19.5 96.2	32.8 93.8	140.1 98	234.9 96.8	329.6 95.5
RECTIFIER TYPE (IR)	40HFL100S02 251UL100S15					

TABLE 5
INVERTER-FED RECTIFIERS - PHYSICAL AND COOLING PARAMETERS

Point Design #	1	2	3	4	5	6
POWER MW	0.5	0.5	0.5	7.0	7.0	7.0
VOLTAGE KVDC	40	40	40	80	80	80
FREQUENCY KHZ	5	15	25	5	15	25
DRY WEIGHT 1b. WET WEIGHT 1b. VOLUME ft ³ DENSITY 1b/ft ³	157	157	157	1374	1374	1374
	169	169	169	1440	1440	1440
	6.75	6.75	6.75	50	50	50
	25.0	25.0	25.0	28.8	28.8	28.8
TOTAL HEAT LOSS kW COOLING AIR 20°C AMB. GPM \$\Delta\$ P PSI \$\Delta\$ T C° (DIODE JUNCT. TEMP. °C)	11.2	19.5	32.8	140.1	234.9	329.6
	6.0	6.0	12.0	24	24	36
	2.0	2.0	8.0	3.8	3.8	5.6
	6.5	12.3	10.0	21.8	36.8	34.7
	(54.0)	(76.0)	(100.0)	(81.0)	(123.0)	(145.0)

2.3 Inverters

In general, SCR inverters are categorized according to the means that is used to commutate or "turn off" the SCRs which are being used as switches to alternately reverse the polarity of a dc power source to an ac load.

Since the weight and volume of the inverter subsystem are determined primarily by the choice of components, packaging and cooling techniques, rather than by the particular circuit concept, the ready availability of hardware experience plus computer software favored the selection of the parallel commutated inverter in this study.

2.3.1 The Parallel Commutated Inverter

The parallel commutated inverter is a sinewave inverter. A sinewave is insured by choosing the characteristic impedance of the resonant components to be sufficiently less than the load impedance to guarantee oscillation. Typically, a circuit is run at a Q of approximately five. The term "parallel" in the inverter nomenclature refers to the position of the capacitors in the resonant circuit relative to the load.

In the simplified schematic of Figure 4, when SCR $_1$ is triggered, current flows sinusoidally through L_1 into C_2 and C_1 . The two capacitors are usually equal and effectively connected in parallel with each other through the low source impedance of the "DC $_{1N}$ " power supply, since the power supply output capacitor $C \gg C_1$. The resonant frequency is determined by L_1 and $C_1 + C_2$. The load is connected in parallel with the commutating capacitors. Once the capacitors are peak charged, current will flow back through L_1 via the diode D_1 . Triggering SCR $_2$ will produce a similar action in L_2 .

Regulation is achieved, that is, power to the load is varied, by changing the time that SCR_2 is triggered relative to triggering of SCR_1 . For example, when D_1 is conducting, the voltage at the junction of C_1 and C_2 is greater than Vdc/2. Triggering SCR_2 at this time will produce greater than normal current in L_2 which in turn will charge C_1 and C_2 to a greater than normal peak negative voltage, thereby increasing the peak-to-peak voltage of the sinewave output. Since the load is connected to this point, the load power will increase proportionately. If the triggering of SCR_1 intrudes on the conduction of D_2 , a similar result will occur in the positive direction.

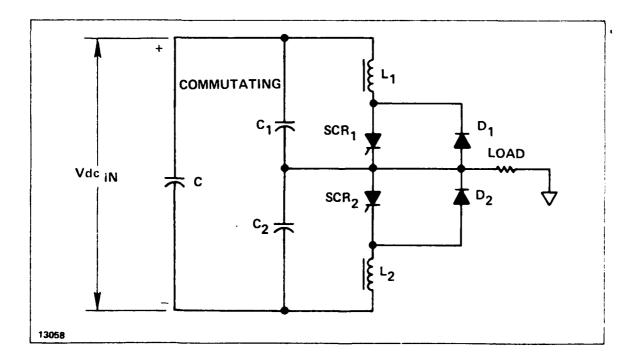


Figure 4 - Parallel Commutated Inverter

The parallel commutating inverter shown in Figure 5 is comprised of two inverters of the type shown in Figure 4 with the load connected in series between the inverters but in parallel with the commutating capacitors of each.

Four additional components are used in each section of this configuration. A saturable reactor (L_S) controls the di/dt applied to the SCR and diode. A damping resistor R_D damps the ringing of the saturable reactor once the diode has stopped conducting. A snubber network consisting of a resistor (R_{SN}) and a capacitor (C_{SN}) controls the rate of reapplied voltage (dv/dt) across the SCR. The coupling capacitor (C_C) is used to prevent inverter failure in the event of a load short circuit.

Regulation is achieved in the bridge inverter by varying the phase shift of side B relative to side A. Both halves of the inverter are resonant at the same frequency. If both sides are in phase, the voltage impressed across the transformer will be zero; conversely, if both sides are 180 deg out of phase, maximum voltage will be impressed across the transformer. In a typical mode of operation both halves of the parallel commutating bridge inverter are started up in phase. The phase of side B is slowly delayed relative to side A until the desired rectified dc output voltage is achieved. Maximum phase shift allowed is usually 144 deg since this will produce 95 percent of the maximum available voltage. Increasing the phase shift the final 36 deg produces only 5 percent increase in voltage and can lead to regulator stability problems, whereas decreasing the phase shift 36 deg to 108 deg produces 14 percent decrease in voltage and is more easily controllable. Varying the phase between 97 deg and 144 deg will handle the normal \pm 10 percent line variations usually encountered by this type of regulator.

2.3.2 Preliminary Inverter Designs

Design points were chosen to explore the minimum and maximum input voltages and the low, medium, and high points of the SCR frequency. A circuit current limit of 1000A rms was chosen based on our understanding of SCR rating and current densities which are reasonable for magnetic components, capacitors and connectors. This current level could be sustained at 5 kHz but was SCR-limited at the higher frequencies.

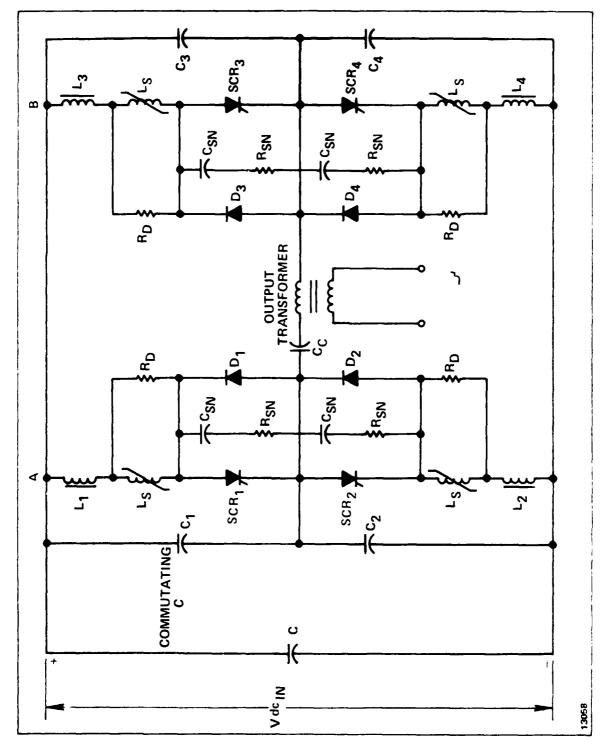


Figure 5 - Parallel Commutated Bridge Inverter

Discussions with several capacitor manufacturers led to the conclusion that there is insufficient experience and data to describe commutating capacitors which are lightweight and low volume and take advantage of the reduced life requirements of the subsystem in this study. Therefore, the capacitor parameters were based on work reported by Gilmour in 1977⁽¹⁾ with the following additional provisions:

- Capacitor unit rms currents were limited to 175A by single bushing capabilities.
- Resistive losses were added and estimated to be of the same order as the dielectric losses.

From the considerations of the dissipation factor and frequency characteristics, a dielectric system of polypropelene/silicone oil was assumed for the capacitors. This dielectric system has been found to be particularly advantageous for frequencies greater than 10 kHz, and the dissipation factor (0.001 at 10 kHz) is essentially uniform out to 25 kHz. Allowing for resistive losses and an operating time of five min resulted in an estimated capacitor energy density of 2.75 joules/lb at 10 kHz which is about one-third the density reported in reference 1 for two min operation, neglecting resistive losses.

The inverter design approach utilized existing computer software to determine parameter values for the circuit shown in Figure 5. Six design points which span the frequency range and input voltage range are listed in Table 6. For 1 kV inputs the SCR configurations are reasonable but module power drops to only 200 kW as the frequency is increased to 25 kHz. At 28 kV input the required number of series SCRs becomes impractical.

Weights and volumes for realizable design points are given in Table 7. The minimum weight designs are air-insulated and utilize both air and water for cooling. Minimum volume designs are immersed in oil for voltage insulation and utilize water plus the heat capacity of the oil for cooling. Consequently the larger spacings required in air increase the volume of the air-insulated designs. Similarly, the weight of the oil nearly doubles the weights of the minimum volume designs as the price for the closer spacing afforded in the liquid dielectric.

⁽¹⁾ A. S. Gilmour, Jr., "Power Conditioning Systems for High-Power, Airborne, Pulsed Applications", IEEE Trans. on Aerospace and Electronic Systems, Vol. AES-13, p. 660 (Nov. 1977).

TABLE 6
INVERTER DESIGN PARAMETERS

		1 k	v			28	kV		Available Recovery
Freq kHz	I RMS	Power Mw	SCR Type	No. SCR	I RMS AMP	Power Mw	SCR Type	No. SCR	Time µs
5	1000	0.81	<u>w</u> T9GH081132DH	4	1000	22.1	AS For 1 kV	72	50
10	770	0.52	W-CODE R270CH06 FNO	4	770	15.7	AS For 1 kV	92	25
25	300	0.20	G.E. C444M	4	300	6.1	AS For 1 kV	97	10

TABLE 7
INVERTER PRELIMINARY DESIGN SUMMARY

		, 		
POWER MW	0.5	0.5	0.5	0.5
VOLTAGE kV	1	1	1 5	1
FREQUENCY kHz	5	10		10
	MIN. WT.	MIN. WT.	MIN. VOL.	MIN. VOL.
DRY WEIGHT 1b.	613	431	1120	711
	1			711
WET WEIGHT 1b.	625	443	1132	723
VOLUME ft ³	23.94	14.81	14.36	8.89
UENSITY lb/ft3	26.1	29.9	78.8	81.3
TOTAL HEAT LOSS kW	50.3	42.3	50.3	42.3
AIR - 20°C AMB.				
CFM	900	148	_	_
Δ T, C ^O	20	20	_	_
Δ P, In-H ₂ 0	0.5	0.5	-	-
WATER - 20°C - AMB.				
GPM	5	5.34	5	5.34
Δ Τ, C ^O	20	20	20	20
Λ P, PSI	10	10	10	10
····				

2.4 Pulse Forming Network

The term "Pulse Forming Network (PFN)" in this study includes all of the elements of a line type modulator such as charge and discharge switches as well as the lumped-element delay line commonly known either as a PFN or a pulse-forming line (PFL).

The design concept employed in this study is the line modulator with sequential charging shown schematically in Figure 6. Although the figure illustrates a complete pulse power conditioning system, the PFN subsystem designs include only those elements starting with the command charge switch and ending with the thyratron and its accessories.

For the majority of the point designs several PFL/thyratron modules are required, a feature which leads easily to the concept of sequentially charging individual modules or groups of modules in order to smooth the load on the prime power. This concept also keeps charging switches and chokes at reasonable sizes. The most influential elements of the PFN subsystem are, as one might expect, the switches and capacitors.

2.4.1 Output Switches

Because of the range of repetition rates required in this study it is straightforward to choose thyratrons as the output switches over other alternatives such as spark gaps. The EG&G HY-7 (MAPS-40) tube represents the state-of-the-art in conventional thyratrons with a normal di/dt range. Parameter ranges of the HY-7 have been expressed in nomograph form in Figure 7. The limit line of the chart simultaneously defines both the peak and average power limitations of the HY-7. The maximum peak power delivered to the load through a single HY-7 is given by:

$$P_0 = 1/2 I_{PK} V_{PK} = (1/2)(40 kV) (50 kA) = 1000 MW$$

The maximum average power P_{av} delivered to the load through a single HY-7 is one megawatt which is the same as delivering the maximum peak power above at 0.1 percent duty.

For example, at a pulse duration τ of 10 μ sec, the maximum capabilities of the HY-7 limit the peak energy to 10 kJ (peak power limitation) and the pulse repetition frequency (PRF) to 100 pps (average power limitation). These limits are illustrated as follows:

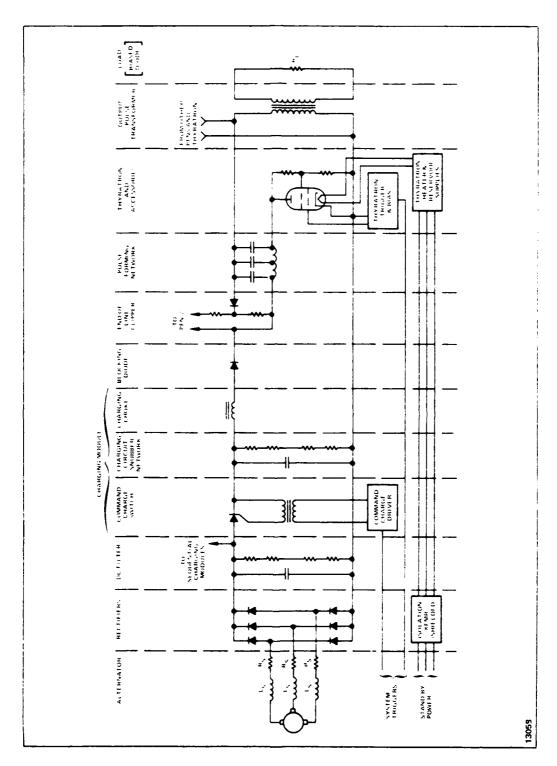


Figure 6 - Line Type Modulator Concept with Sequential Charging

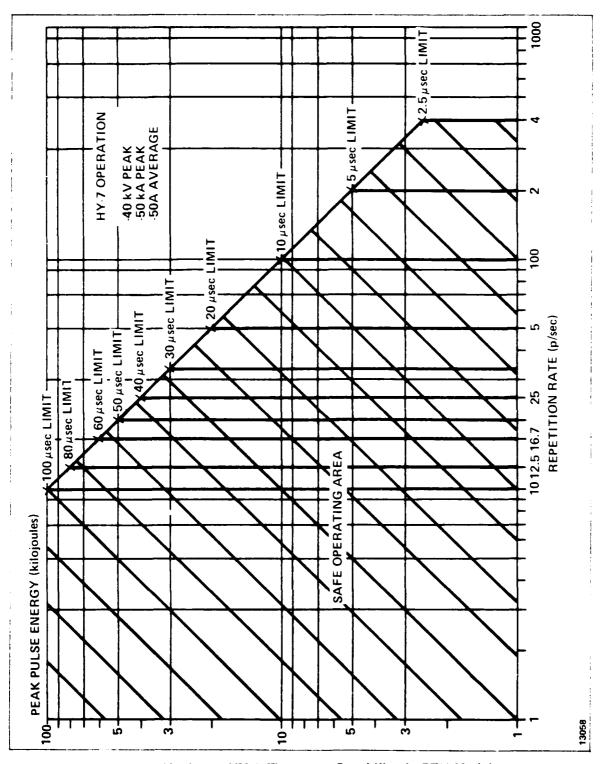


Figure 7 - Maximum HY-7 Thyratron Capability in PFN Module

Peak Energy =
$$P_0^T$$
 = (1000 MW) (10⁻⁵ sec) = 10 kJ
PRF_{max} = $\frac{P_{av}}{P_0^T}$ = $\frac{10^6 \text{ W}}{10^4 \text{ J}}$ = 100 pps

The safe operating area presented in the nomograph is based upon the full utilization of the peak and average power capabilities of the HY-7. Referring to the above example, if a 10-usec pulse of only 5 kJ were used, then the average power capability would allow a maximum PRF of 200 pps. That is, one can move along the limit line only toward reduced peak energy per pulse.

The number of HY-7 thyratons required by a particular set of parameters may be determined either by the peak or average power limitation. The nomograph is simply a tool to simplify analysis so that the maximum utilization of the switches at their simultaneous peak and average power capabilities may be achieved in a system under design thereby optimizing the system with respect to the switches.

2.4.2 PFL Capacitors

Typically, the PFL capacitors make up a substantial portion, say 25 percent, of the weight of a PFN subsystem. A strong factor in the design therefore is the allowable density at which energy can be stored in these capacitors. This energy density in turn is determined by the voltage stress which can be withstood by the capacitor dielectric while maintaining an adequate lifetime.

Recent development programs at Maxwell (2) and Hughes (3) have indicated the feasibility of pulse capacitors in the 60 to 80 J/lb range operating in bursts of 30 to 120 sec.

Since the operating time of 5 min was required during Phase I, consideration of the additional heat built-up and long thermal time constants of such components led to the decision to derate the capacitor energy density to 35 J/lb.

^{(2) &}quot;High-Energy Density Pulse-Forming Network and Continued Capacitor Testing", Final Report on Contract DAAK40-77-C-0118, by Maxwell Laboratories, Inc. San Diego, Calif. (April 1980).

^{(3) &}quot;Capacitors for Aircraft High Power", Final Report on Contract F33615-75-C-2021, by Hughes Aircraft Co., Culver City, Calif. (January 1980).

2.4.3 End-of-Line Clippers

The series diode and resistor assemblies which terminate the PFLs to absorb inverse voltage transients are devices whose parameters are not critical for pulse generator performance. The critical parameter is the associated tolerance of the thyratron switch for inverse voltage. For the HY-7 operating at full power, it has been found that the inverse voltage should be restricted to about 1000 V to avoid arcing. However, an inverse of 500 V is required to ensure turnoff. Thus, the clipper resistors must essentially match the PFL impedance and the diode assemblies must be constructed of fast turn-on diode devices in a low-inductance configuration. Presently available diode assemblies can turn on in about 1.5 μ sec, although the individual devices operate much faster. A turn-on time of 0.5 μ sec would be more compatible with the HY-7 requirements.

The technique of Levy and Creedon ⁽⁴⁾ was used to derive a peak current rating from published average current ratings of diodes. A ratio of 300:1 is suggested for the maximum single-shot 10 µsec current pulse to diode rated average current, based on destructive testing. Thus a 100A diode would be rated for a 30 kA pulse, without a safety factor. For the purposes of this study, safety factors of four in current and 1.5 in voltage have been utilized. Maximum operating peak clipper currents are 7 to 8 kA and the maximum operating voltage is 40 kV.

Variations in mismatch between the PFN and its load impedance will affect the clipper component requirements as well as overall dissipation. For the purpose of this study a 25 percent load mismatch was assumed. The effects of various load mismatches on the reflected voltage and energy are plotted in Figures 8 and 9.

⁽⁴⁾ S. Levy and J.E. Creedon, "Solid State Clipper Diodes for High Power Modulators", IEEE Conf. Record of the 1978 Thirteenth Pulse Power Modulator Symposium, pp 60-65 (June 1978)

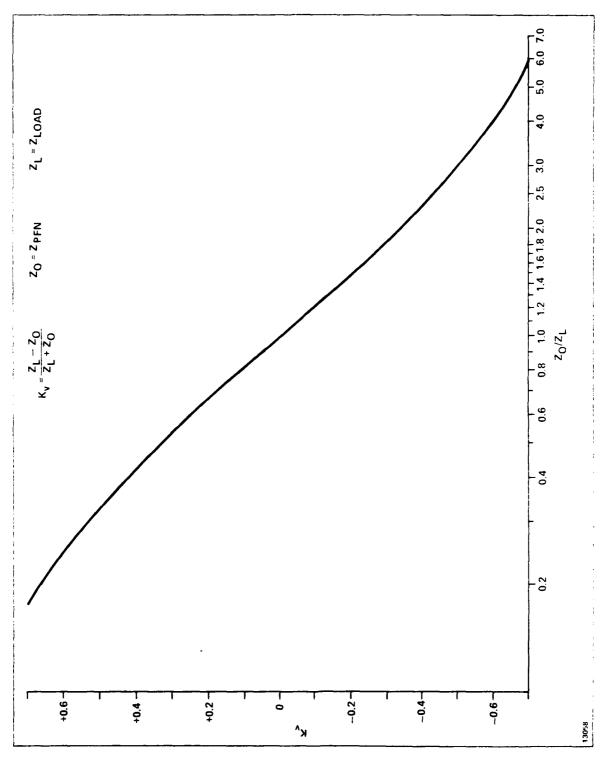


Figure 8 - Voltage Reflection Coefficient

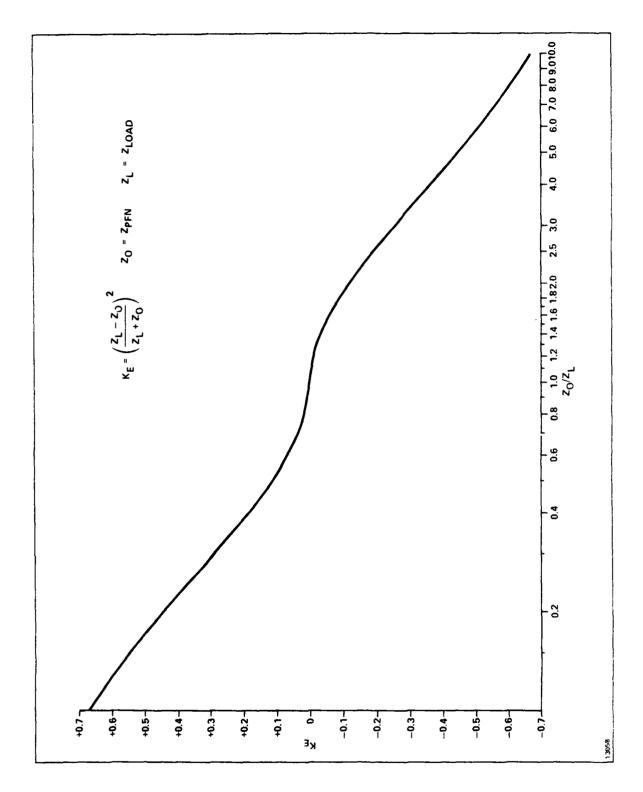


Figure 9 - Energy Reflection Coefficient

2.4.4 PFN Preliminary Design Points

The six design points chosen from the range of interest are listed in Table 8. Selection of these points is based on the following rationale:

TABLE 8
PFN PRELIMINARY DESIGN POINTS

Design Point	Average Power (MW)	Energy Per Pulse (kJ)	PRF (Hz)	Pulse Width (µs)	Charge Mode
1.	0.5	10	50	10	Inverter
2.	7.0	25	280	20	Inverter
3.	7.0	25	280	20	Sequential
4.	14.0	100	140	5	Sequential
5.	14.0	50	280	5	Sequential
6.	30.0	100	300	40	Sequential

Design Point 1 - This 0.5 MW point can utilize no more than one HY-7 thyratron, thereby ruling out sequential charging. An inverter charging circuit is used to maintain constant loading of the power supply.

Design Points 2 and 3 - Both sequential and inverter charging are evaluated for a single design point at a significant power level which could become a building block for higher power systems.

Design Points 4 and 5 - These 14 MW points which differ in pulse energy and PRF are examined to illustrate the effect of HY-7 average power utilization.

Design Point 6 - This point represents the maximum power in the range of interest and may be accomplished by combining several 7-MW modules.

The various pulse durations are covered by the configurations of pulse forming lines and thyratrons shown in Figure 10. An artist's concept of a basic PFN module using two thyratrons and a single charging circuit is shown in Figure 11.

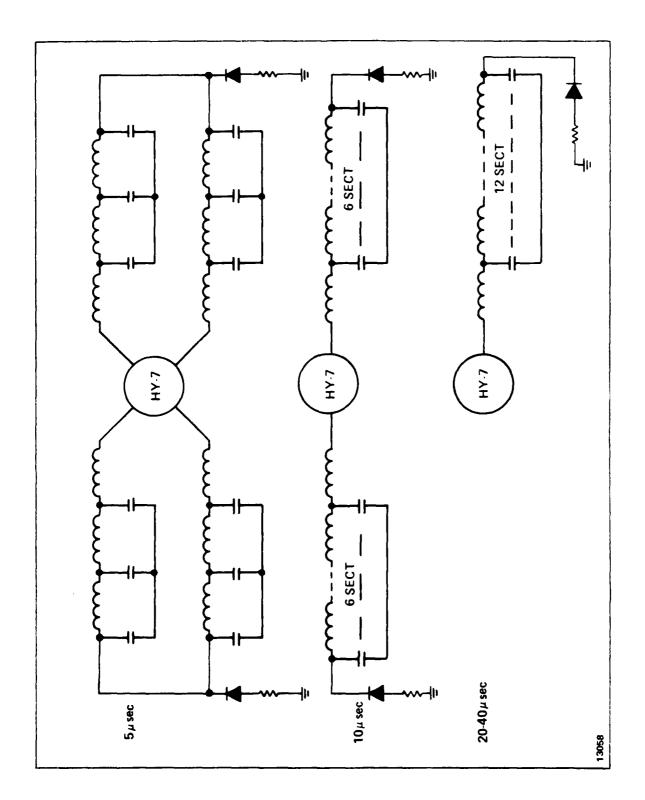


Figure 10 - Typical PFN Configurations

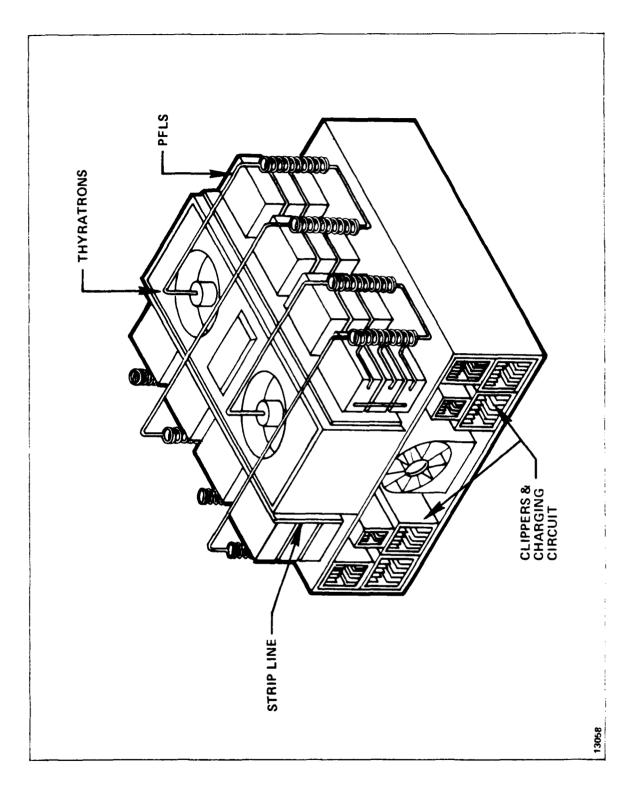


Figure 11 - PFN Module Two Thyratrons with Charging Circuit

Summaries of the preliminary PFN design data for the six points described above are given in Tables 9 through 12. In deriving these results, cooling systems have been designed to dissipate the maximum heat loss which would have been encountered with a badly mismatched load. However, efficiencies have been calculated assuming a matched load.

2.5 Critical Device Parameters

The preliminary design phase of this program has revealed a number of device parameters which limit not only the attainment of light weight and low volume but also the feasibility of certain design points altogether. Although these parameters have been discussed in previous subsystems, the following summary comments are added for emphasis.

In the case of the two rectifier subsystems, the most influential parameter by far has been found to be packaging of SCR and rectifier components. To some extent this aspect of device construction also affects the turn-on capability of end-of-line-clipper diodes which must be grouped in assemblies whose inductance slows the operation greatly, relative to the basic device capability.

Inverter designs over the range of interest in this study have been severely limited by the voltage, current, and frequency capabilities of SCRs. Similarly, data on appropriate capacitors and magnetic components have been of limited applicability. These limitations have been partially addressed in Phase II by designing suitable magnetic components. In the case of commutating capacitors, the following situation prevails:

- The technology is mature for capacitors requiring 10 years life, but manufacturers are reluctant to advise on energy densities which might be attained for only 100 hours life.
- Manufacturers require very specific capacitor requirements before responding concerning size, weight and feasibility.
- Water-cooled capacitors, though attractive for high powers, are strictly limited in voltage rating and prohibitively large.

Pulse capacitors and thyratron peak power capability directly influence the size and weight in the PFN design. Plausible energy densities at modest repetition rates appear to have topped out around 80 J/lb for operating bursts up to 2 min. As illustrated

TABLE 9
PFN SUMMARY - MINIMUM WEIGHT

Point Design						
Number	1	2	3	4	5	6
Power MW	0.5	7.0	7.0	14.0	14.0	30.0
Energy/Pulse kJ	10	25	25	100	50	100
Rep. Rate Hz	50	280	280	140	280	300
Pulse Length µs	10	20	20	5	5	40
Charge Method	INV.	INV.	RES. CH.	RES. CH.	RES. CH.	RES. CH.
		- 111				
Dry Weight 1b.	1455	9990	4004	11,379	7350	15,122
Wet Weight 1b.	1507	10,648	4324	12,339	7990	16,402
Volume ft ³	70.32	423	200	635	420	787
Density	21.4	25.2	21.6	19.4	19.0	20.8
(WET) lb/ft ³						<u> </u>
i .						
PWR/VOL kW/ft	7.11	16.55	35.0	22.05	33.33	38.12
PWR/WT kW/lb.	0.33	0.66	1.62	1.13	1.75	1.83
}						
Heat Loss kW	75.7	967	248	538	447	888
(Matching Load)				!		
Efficiency	87	88	97	96	97	97
(max.) î					L	

TABLE 10
PFN SUMMARY - MINIMUM VOLUME

Point Design Number	1	2	3	4	5	6
Power MW	0.5	7.0	7.0	14.0	14.0	30.0
Energy/Pulse kJ	10	25	25	100	50	100
Rep. Rate Hz	50	280	280	140	280	300
Pulse Length us	10	20	20	5	5	40
Charge Method	INV	INV.	RES. CH.	RES. CH.	RES. CH.	RES. CH.
Dry Weight lb.	2983	20,435	7808	25,056	15,317	29,358
Wet Weight 1b.	3030	20,961	8108	25,968	15,917	30,558
Volume ft ³	43.32	280	122	406	239	462
Density lb/ft ³	69.9	74.9	66.5	64.0	66.6	66.1
PWR/VOL kW/ft3	11.54	25.00	57.4	34.48	58.58	64.94
PWR/WT kW/lb.	0.16	0.33	0.86	0.54	0.88	0.98
	}				}	
Heat Loss kW	75.7	967	248	538	447	888
(Matching Load)		1				
Efficiency	87	88	97	96	97	97
(max.) %						

TABLE 11
PFN - MIN. WEIGHT - PHYSICAL AND COOLING PARAMETERS

Point Design Number	1	2	3	4	5	6
Power MW Energy/Pulse kJ Rep. Rate Hz Pulse Length µs Charge Method	0.5 10 50 10 INV.	7.0 25 280 20 INV.	7.0 25 280 20 RES. CH.	14.0 100 140 5 RES. CH.	14.0 50 280 5 RES. CH.	30.0 100 300 40 RES. CH.
Dry Weight lb. Wet Weight lb. Volume ft ³ Density lb/ft ³	1455 1507 70.32 21.4	9990 10,648 423 25.2	4004 4324 200 21.6	11,379 12,339 635 19.4	7350 7990 420 19.0	15,122 16,402 787 20.8
Heat Loss - kW MAX. MIN.	115.7 75.7	1367 967	648 248	1338 538	1247 447	2488 888
Air - 20°C AMB. CFM @ 0.5 in-H ₂ 0 T - C°	1138 39	8971 40	8950 39	20,159 39	16,990 39	33,972 39
Water - 20°C AMB. GPM at 4 PSI T - C°	12.43 24	147 26	40.35 40	82 4 0	81.5 40	161.4 40

TABLE 12
PFN - MIN. VOLUME - PHYSICAL AND COOLING PARAMETERS

Point Design Number	1	2	3	4	5	6
Power MW Energy/Pulse kJ Rep. Rate Hz Pulse Length µs Charge Method	0.5 10 50 10 INV.	7.0 25 280 20 INV.	7.0 25 280 20 RES. CH.	14.0 100 140 5 RES. CH.	14.0 50 280 5 RES. CH.	30.0 100 300 40 RES. CH.
Dry Weight lb. Wet Weight lb. Volume ft ³ Density lb/ft ³	2983 3030 43.32 69.9	20,435 20,961 280 74.9	7808 8108 122 66.5	25,056 25,968 406 64.0	15,317 15,917 239 66.6	29,358 30,558 462 66.1
Heat Loss - kW MAX. MIN.	115.7 75.7	1367 967	648 248	1338 538	1247 447	2438 888
Air - 20°C AMB. CFM @ 0.5 in-H ₂ 0 ΔT - C°	-	-	-	-	-	-
Water - 20°C AMB. GPM at 4 PSI Δ T - C°	8.36 30	120 25	38 40	76 40	76 4 0	152 4 0

in Figure 7, the limited peak power capability of the HY-7 results in a much larger number of thyratrons for short pulse systems having the same average power as associated longer pulse systems. Thyratrons with five-fold increased peak power capability, such as the HY-7160, are under development.

In addition, the extreme sensitivity of the HY-7 thyratron to reverse voltage places a burden on both the clipper design and the ultimate load selection. Further improvements in the HY-7 inverse holdoff capability, plus development of a megawatt class double-ended thyratron, would aid in reducing the requirement for matched clippers with full pulse current rated diodes.

Finally, the development of so-called "quick-start" or "cold-cathode" thyratrons would eliminate the requirement for auxiliary power and filament transformers weighting about 30 lb each.

3. THREE PHASE RECTIFIER - PHASE II

The objective of this phase was to make detailed electrical and mechanical designs of a three phase SCR rectifier system using present state-of-the-art components. These components were to be selected from the preliminary design work done in Phase I.

3.1 Electrical Design

3.1.1 Design Points

The design points for the rectifiers are as specified in Table 13. The following assumptions have been made:

- 1) The source regulation of \pm 5 percent is a requirement on the generator which drives the rectifier. The generator could vary as much as \pm 5 percent no-load to full load.
- 2) The ± 5 percent variation described above will have a 40 msec recovery time. This is also a requirement on the generator.
- 3) The load on the rectifier is expected to be inductive and therefore have a lagging power factor.

3.1.2 Design Philosophy

After inspection of the voltage levels specified as design points, 1 kV, 50 kV, 100 kV, 150 kV, 200 kV, it became apparent that the design could be most easily handled in modular form. That is, two basic voltage level modules would be designed, a 1 kV module and a 50 kV module. The 100 kV, 150 kV, 200 kV points would be achieved by "stacking" 50 kV modules. The basic 1 kV module would be designed at the 0.5 MW level. Higher power levels at 1 kV would be achieved by adding additional 0.5 MW modules in parallel. This approach would minimize the types of devices required.

TABLE 13
RECTIFIER DESIGN POINTS

P	f	v	P	f	v	P	f	v
1	1	1	2	4	3	4	2	5
1	1	2	2	4	5	4	4	1
1	1	3 -	. 3	1	1	4	4	3 ;
1	1	4	3	1	2	4	4	5
1	1	5	3	1	3	5	1	1 :
1	2	2	3	1	4	5	1	2
1	2	5	3	1	5	5	1	3
1	3	2	3	2	2	5	1	4
1	3	4	3	2	4	5	1	5
1	4	2	3	3	2	5	2	2
1	4	4	3	3	4	5	2	4
1	5	1	3	4	2	5	3	2
1	5	2	3	4	4	5	3	4
1	5	3	3	5	1	5	4	2
1	5	4	3	5	2	5	4	4 1
1	5	5	3	5	3	5	5	1
2	2	1	3	5	4	5	5 5	2
2	2	3	3	5	5	5		3
2	2	5	4	2	1	5	5	4
2	4	1	4 	2	3	5	5	5
Three	phase rec	tifier						
F	$P_1 = 0.5MW$ $P_2 = 7MW$ $P_3 = 14MW$ $P_4 = 21MW$			$f_1 = 200H$ $f_2 = 600H$ $f_3 = 1.2k$ $f_4 = 1.8k$	Iz :Hz		$V_1 = 1kVd$ $V_2 = 50kV$ $V_3 = 100k$ $V_4 = 150k$	dc Vdc
F	mbers abo	ve shall	be interr	$f_5 = 2.5k$	Hz		$V_5 = 200k$	Vdc

3.1.3 Component Selection

(f), and output voltage (V).

The SCR rectifiers used were selected from the group researched in Phase I. The prime parameters considered were P.I.V., recovery speed and forward current capability. Of the types explored in Phase I, the General Electric C-613 SCR seemed most suitable.

This device is capable of high frequency, (up to 5 kHz), high voltage, (2000 V), high current (750A rms), and is packaged in the hockey-puck style. This device was used in all design points. Although the C-613 appears to be grossly overrated with respect to current level in some of the design points, no other more suitable device was found. Figure 12 shows the SCR operating rms levels of current at all voltage and power levels. The block in the upper right corner shows the multiplier to be used at various control retard angles. This factor will be insignificant in the region of normal control angles.

3.1.4 Design

The results of the concept of a modular approach were two basic modules utilizing the C-613 SCR. One module designed for the 1 kV output at the 0.5 MW level is shown in block diagram form on Figure 13. This module consists of six C-613 SCRs arranged in the three-phase bridge configuration with one SCR and its trigger circuit in each of the six legs.

Figure 14 shows the basic 50 kV module. This module consists of six legs; each leg contains 60, C-613 SCRs, with associated trigger circuits and voltage balancing networks in series.

3.1.4.1 Series Compensation

The SCRs do not have matched characteristics; therefore, it is necessary to provide compensation to aid in balancing the voltage applied during the reverse recovery and after recovery.

3.1.4.1.0 Recovery Compensation

The recovery time of a rectifier (SCR) is a characteristic of the particular device and is dependent on certain operating conditions; namely, the junction temperature, the forward conducting current, IFM, prior to commutation and the rate of fall of conducting forward current, A/ μ sec. Curves relating these parameters to the maximum recovered charge, Q_{max} , in microcoulombs are generally given on the manufacturer's data sheets for the particular device. The generally accepted method of equalizing the voltage division during recovery of a string of rectifiers (SCRs) is to put a capacitor across each device to

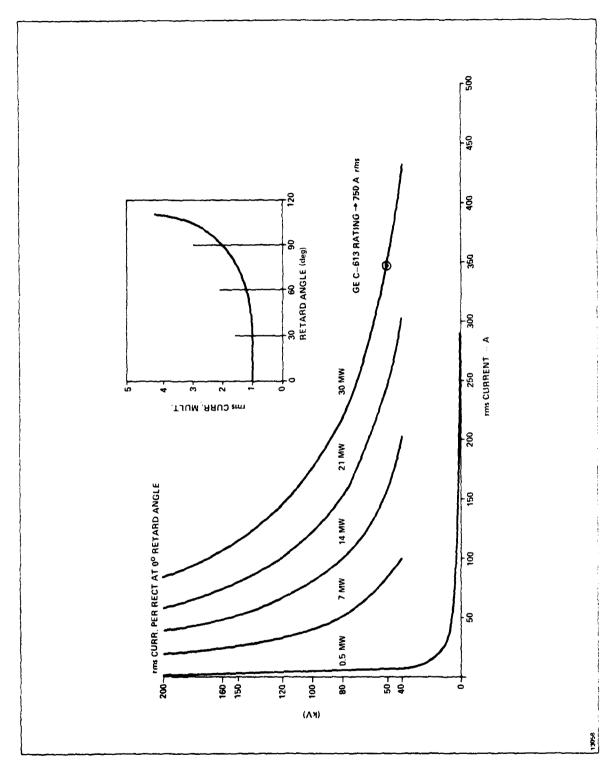


Figure 12 - SCR Operating Levels

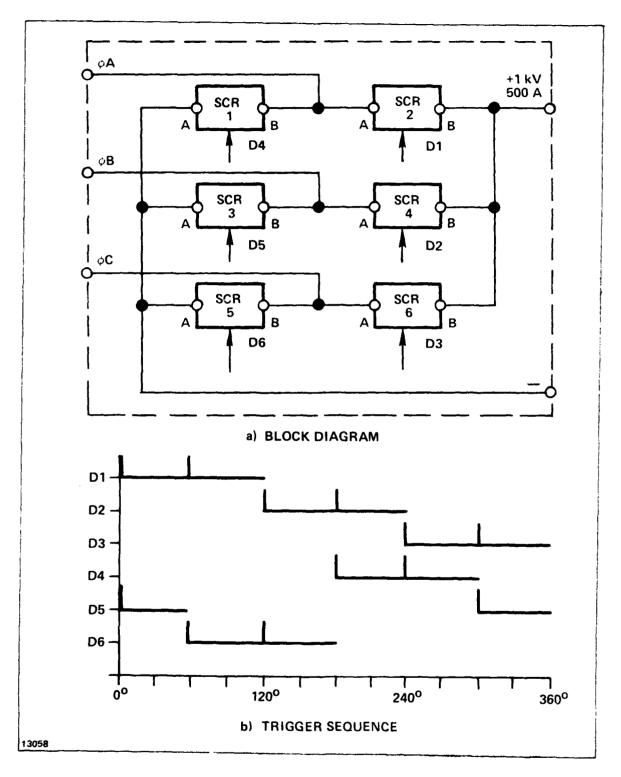


Figure 13 - Basic I kV Module

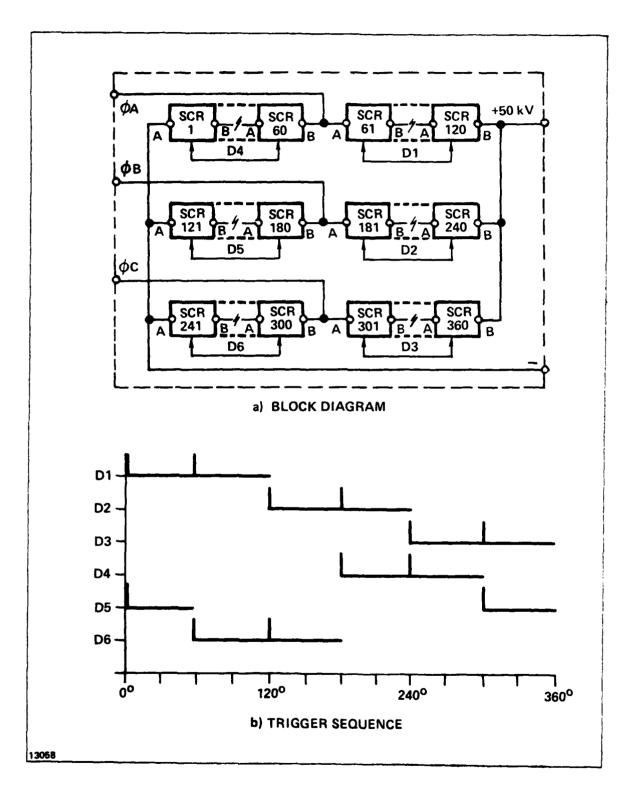


Figure 14 - Basic 50 kV Module

minimize the effect of unequal stored charge. These capacitors, in the case of SCRs, generally will have a fair amount of energy stored in them prior to forward conduction of the SCR. A limiting resistor is used in series with the capacitor to prevent excessive surge current during "turn-on" of the SCR. The maximum voltage difference that will appear across a device is $\Delta V max$, where $\Delta V max = \Delta Q max/C$. Worst case junction temperature, operating forward current levels, IFM, and rate of fall of forward current, in $A/\mu sec$, were used to determine the capacitor values. The capacitor was chosen to limit $\Delta V max$ to +20 percent.

3.1.4.1.1 Leakage Current Compensation

Since all rectifiers, including SCRs, have some reverse resistance, they will have some reverse current with an applied reverse voltage. This resistance or current is a characteristic of a particular device and is temperature sensitive. The manufacturer generally specifies the maximum leakage current at the rated P.I.V. and maximum temperature. Figure 15 is a plot of this characteristic for the General Electric C-613 device.

The equation

$$RS = \frac{ns Ep - Em}{(ns-1) \Delta IR}$$

can be solved for the shunting resistor value (R_1) required to compensate for this leakage current. In the above equation

ns = number of series rectifiers (SCRs)

Ep = maximum voltage desired across a rectifier

Em = total reverse voltage applied to rectifiers

△IR = possible difference in leakage currents

Ep was chosen to be +20 percent of Em/ns; Δ IR was taken as 75 percent of IR at the maximum junction temperature and 50 percent of the rated P.I.V. of the SCR.

Figure 16 shows the maximum operating P.I.V. expected and the percentage of the rated P.I.V.

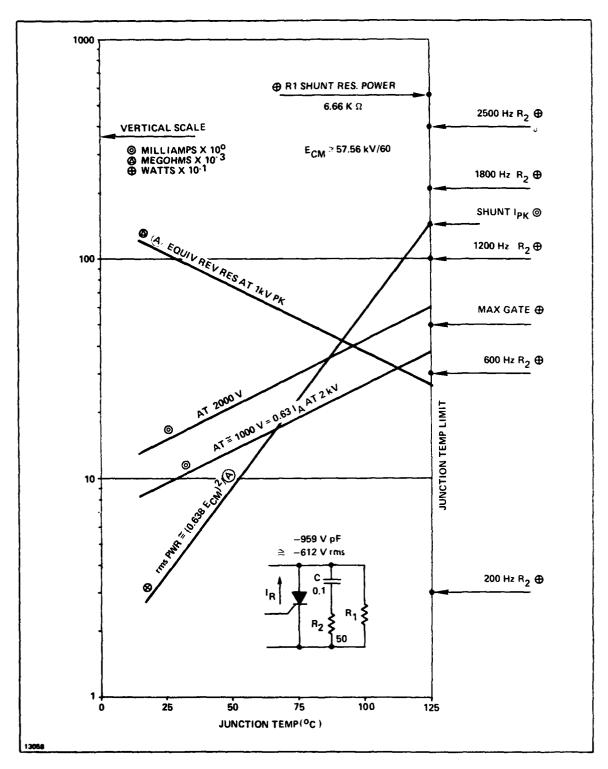


Figure 15 - GE C-613 Maximum Leakage Current

MODULE	MAX PIV AT HI LINE	% RATED PIV AT HI LINE
50 kV	1150 V	58%
1 kV	1153 V	58%

NOTES:

- 1 MAX PIV INCLUDES +20% ALLOWANCE FOR UNEQUAL VOLTAGE DISTRIBUTION IN 50 kV MODULES
- (2) HI LINE IS NOMINAL LINE VOLTAGE +5%

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Figure 16 - Maximum Operating P.I.V.

3.1.5 Power Losses

The power losses in the SCR consists of:

- Forward Conducting Loss This loss is a function of the forward conduction current and the voltage drop across the SCR. These losses are plotted for each rectifier in Figure 17 relative to the operating voltage and power level.
- 2) Reverse Leakage Loss This loss is a function of the reverse leakage current and the operating P.I.V. and is plotted on Figure 17.
- Reverse Recovery Loss This loss is a complex function of the forward current level prior to recovery, the recovery current rate of change in A/µsec, the commutation angle and the retard angle, the recovered charge, the recovery time, the P.I.V. during recovery and the operating frequency. A typical plot of these losses at the 30 MW level for the four output voltage levels and five frequency points is shown in Figure 18.

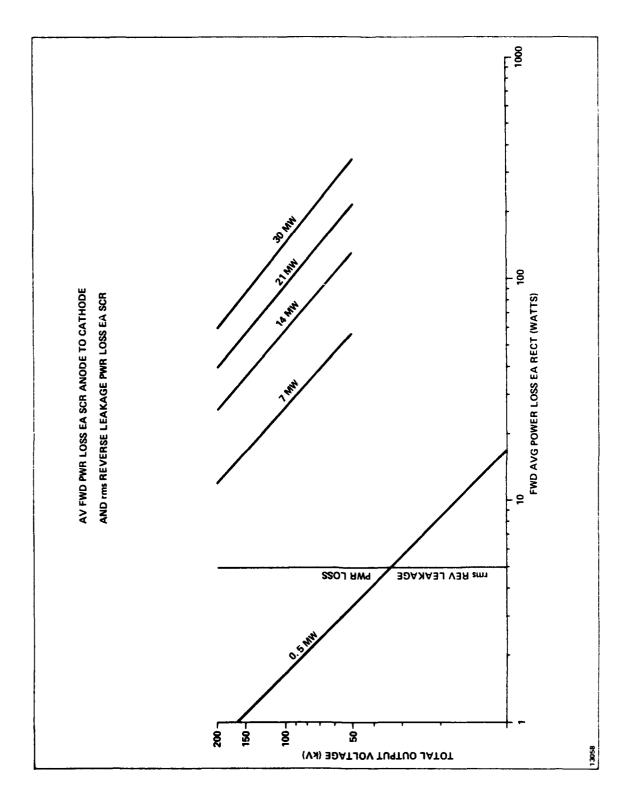


Figure 17 - Forward Conduction and Reverse Leakage Losses

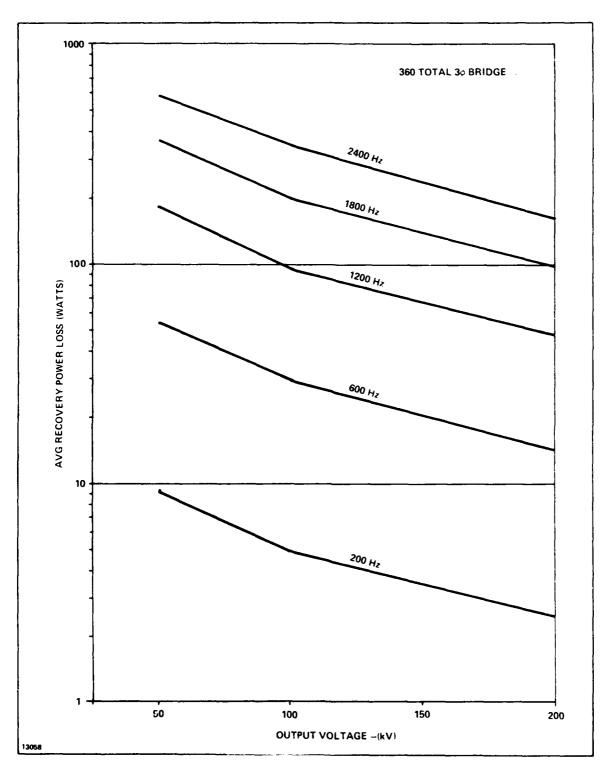


Figure 18 - Reverse Recovery Loss Per SCR at the 30 MW Level

- 4) Gate Loss The average gate loss is in the order of 2.5 W.
- 5) Leakage current compensating resistor This loss is a function of the P.I.V. and is depicted on Figure 15.

3.1.6 Gate Triggering

Each SCR will be accompanied by its own trigger circuit as shown in Figure 19. A portion of the forward hold off voltage of the SCR will be applied to MOSFET Q1 and C1 through the reverse voltage blocking diode CR3. CR1 is a photodiode and will gate Q1 "on" when exposed to a light source from an optical coupling. Q1 will then pass a voltage and current pulse to the gate of the SCR. Figure 19 (D) shows the trigger sequence from the optical source to the PIN diodes. The triggers are shown with no retard angle. When modules are stacked, all respective gates D1-D6 will receive pulses simultaneously.

The light source mentioned above would consist of a light-emitting-diode (LED) mounted in a fiberoptic link/housing such as the Hewlett Packard HFBR-1500/1501. The LED would be driven from a suitable TTL logic gate. The PIN diode or receiver would be mounted in a similar fiberoptic link/housing in the SCR module. Trigger signals would be coupled via the fiberoptic link from the LED transmitter to the PIN diode receiver to gate Q1 "on" thereby firing the SCR.

3.1.7 Design Point Schematics

Figure 20 is a block diagram of the 21 MW, 600 Hz, 100 kV design point. Figure 21 shows the internal circuitry for the modules. This design consists of two 50 kV modules rated at 210A "stacked" on top of each other to obtain 100 kV at 210A. Separate three-phase drive voltage to each module is required in the present concept. However, higher voltage modules could be considered if required to interface directly with higher voltage sources. Since fiberoptic links can be designed to isolate several hundred kilovolts, the trigger isolation would not be a limiting factor.

Figure 22 is a block diagram of the 7 MW, 1.8 kHz, 1 kVdc design point. The blocks 1 through 14 are as shown on Figure 19 (C). The detail of the blocks of Figure 19 (C) are shown on the same figure as A and B.

An output filter is shown in the above schematics for completeness. However, the filter has not been included in the detailed design results and is therefore shown within dashed lines.

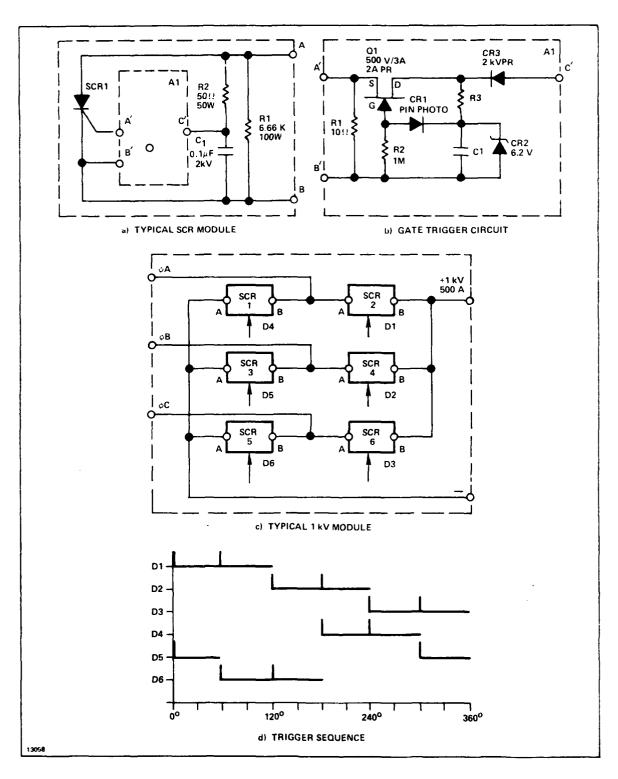


Figure 19 - Gate Trigger Circuit

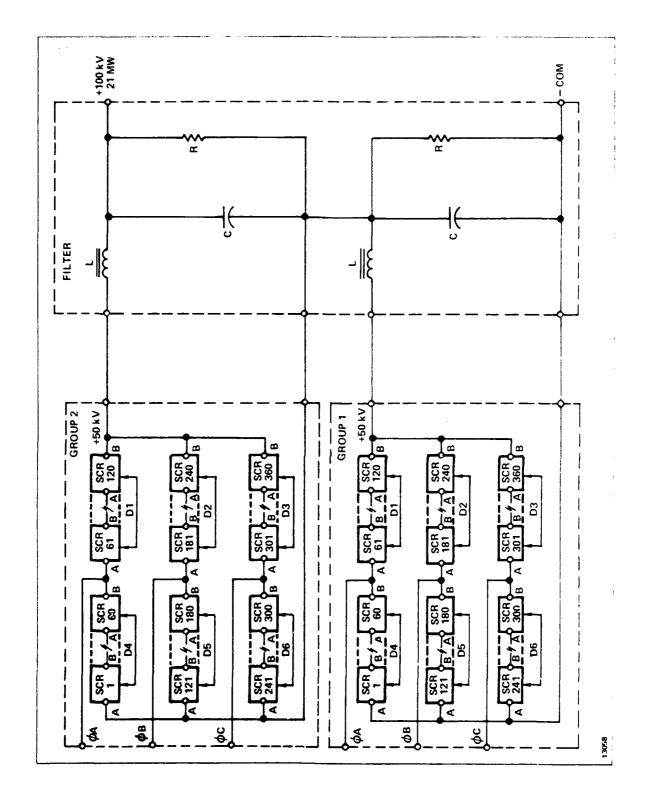
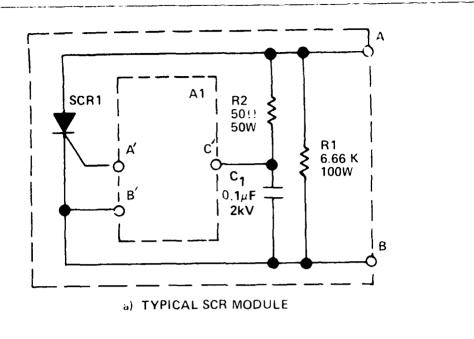


Figure 20 - Design Point Block Diagram 21 MW/600 Hz/100 kV



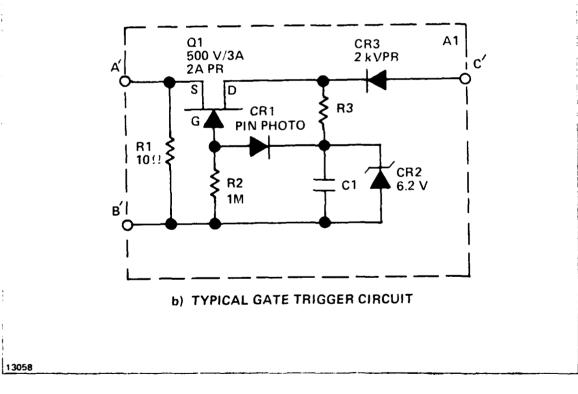


Figure 21 - Design Point Circuits 21 MW/600 Hz/100 kVdc

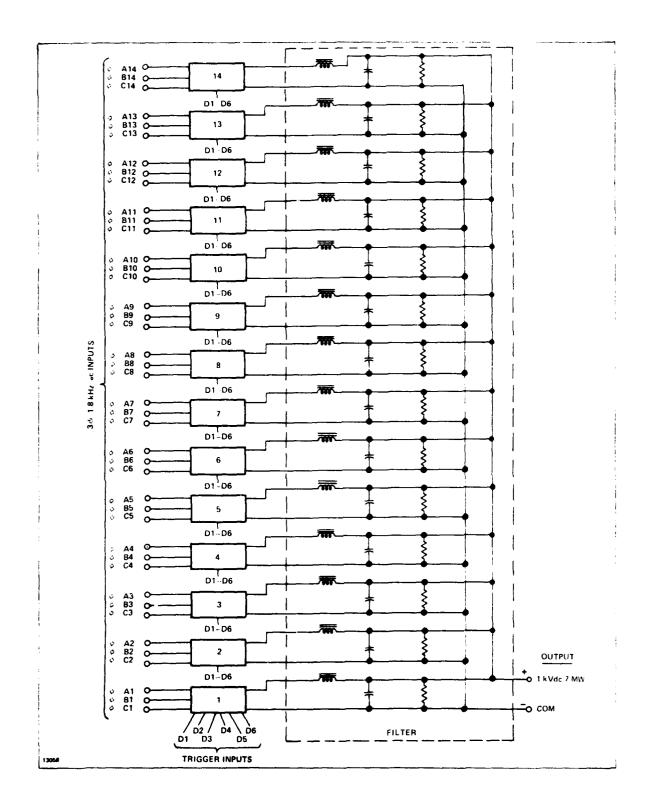


Figure 22 - Design Point Block Diagram 7 MW/1.8 kHz/1 kVdc

3.2 Mechanical Designs

Sixty design points were evaluated for both minimum weight and minimum volume designs. Ambient conditions were assumed to be 20°C and a pressure range of 20.58 to 29.92 in. of mercury, corresponding to an altitude variation from sea level to 10,000 ft. Cooling media included forced air, water and oil. Conventional components, heat sinks and accessories were utilized. No allowance was made for electrical or mechanical interfaces between subsystems, such as high voltage bushings, output filter, etc.

The minimum weight designs are air-insulated with air and water cooling as needed and voltage isolation only at the mounting surface. Minimum volume designs are oil insulated.

The results of the study for the sixty design points are given in Table 14.

4. INVERTER-FED RECTIFIER PHASE II

This section describes the detailed electrical and mechanical designs of a single phase bridge rectifier using present state-of-the art components based on the preliminary design work done in Phase I.

4.1 Electrical Design

4.1.1 Design Points

The design points for the rectifiers are shown in Table 15 of this report. Although the method of modular design yields all 125 possible combinations of parameters, only the specific 60 points shown in the table were considered.

4.1.2 Design Philosophy

The design approach was based on the fact that the output voltages 40, 80, 120, 160, and 200 kV, are multiples of the lowest voltage of 40 kV. Therefore, from a voltage standpoint it seemed practical and logical to "stack" basic 40 kV modules to obtain the various voltage levels.

TABLE 14 "THREE-PHASE RECTIFIER DESIGNS"

							Mini	Minimum Weight	ight					Minin	Minimum Volume	une
	Input	Output														
Average	Fre-	Volt-	Heat		Dry			Air	ΔT		H ₂ 0		ΔP	Dry	Wet	Vol-
Power	quency	age	Load	Eff.	Weight	Weight	Volume	Flow	Air	in-	Flow	Н20	Н20	Weight	Weight	
ME	Hz	kν	¥	æ	1b	qı	ft ³	CFM	ပ	H20	GPM	હ	psi	16	16	£t3
0.5	200	-	1.81	9.66	32	1	1.3	933	5.0	0.2	ı	ı	ì	33	62	0.9
0.5	200	20	28.7	94.6	1430	ı	65.3	3680	20.0	1.0	١	ı	1	1300	2620	38.0
0.5	200	100	56.10	89.9	2860	ı	157.0	7360	19.6	1.0	1	1	_ 	2640	4530	6.99
0.5	200	150	83.5	85.7	4280		236.0	11030	19.4	1.0	ı	ŧ	ı	4090	7180	103.0
0.5	200		110.8	81.8	2680	1	311.0	13240	21.5	9.0	1	ı	ı	5350	9150	132.0
0.5	009	20	30.0	94.3	1430	,	65.3	3680	21.0	1.0	ı	ı	1	1300	2620	380.0
0.5	009	150	86.0	85.2	4280	,	236.0	11030	20.5	1.0	ı	1	1	4090	7180	103.0
0.5	1200	20	33.7	93.7	1430	1	65.3	3680	23.5	1.0	ı	1	ı	1300	2620	38.0
_	1200	150	95.3	84.0	4280	ı	236.0	11030	22.2	1.0	ı	ı	1	4090	7180	103.0
0.5	1800		38.9	95.8	1430	ı	65.3	3680	27.0	1.0	ı	ı	ı	1300	2620	38.0
0.5	1800		108.8	82.1	4280	ı	236.0	11030	25.3	1.0	ı	1	ı	4090	7180	103.0
0.5	2500		5.35	6.86	27.5	28.5	1.3	1	1	ı	1.2	16.9	4.0	33	62	6.0
	2500		47.5	91.3	1430	,	65.3	3680	33.0	1.0	1	1	i	1300	2620	38.0
0.5	2500		89.4	84.8	2860	ı	157.0	7360	31.1	1.0	1	ı	ı	2640	4530	6.99
	2500		131.2	79.2	4280	1	236.0	11030	30.5	1.0	ı	ı	١	4090	7180	103.0
0.5	2500		172.9	74.3	2680	·	311.0	22070	20.1	0.8	1	ı	1	5350	9150	132.0
7.0	009	~	29.5	9.66	384	405.0	16.0	ı	1	T	7.0	15.8	6.5	397	735	10.5
7.0	009	100	80.5	98.8	2970	,	170.0	3460	24.4	1.0	ı	•	1	2640	4530	6.99
7.0	009		136.4	98.1	2680	1	311.0	13240	26.4	9.0	1	ι	1	5350	9150	132.0
7.0	1800	-	54.8	99.5	384	405.0	16.0	ſ	1	1	7.0	29.6	6.5	397	735	10.5
7.0	1800	100	120.1	93.3	2970	1	170.0	8460	36.4		ı	,	ı	2640	4530	6.99
7.0	1800		191.7	97.3	5948	,	338.0	15230	32.3	٠	1	1	1	5350	9150	132.0
14.0	200	-	9.09	9.66	881	ı	37.0	6530	20.0	1.0	ı	ı	1	794	1470	21.0
14.0	200	20	6.97	99.4	2430	1	136.8	9080	21.7	1.5	ı	1		1820	3160	44.7
14.0	200	100	95.3	99.3	2970	ı	170.0	8460	28.9	1.0	ł	ı	<u> </u>	2640	4530	6.99
14.0	200	150	121.7	99.1	4450	ı	256.0	12690	24.6	1.0	i	1	1	4090	7180	103.0
14.0	200	200	148.6	0.66	5940	1	338.0	15230	25.0	•	1	ı	1	5350	9120	132.0
14.0	009	20	86.3	99.4	2430	ı	136.0	0806	24.4	1.5	ı	1	1	1820	3160	44.7
14.0	009	150	134.6	0.66	4450	1	256.0	12690	27.2	1.0	1	1	ı	4090	7180	103.0

TABLE 14 (Cont.)

							Mini	Minimum Weight	aht					Minir	Minimum Volume	ile
	Input	Output								ΔP						
Average	Fre-	Volt-	Heat		Dry	Wet		Air	ΔT	Air	П20 Н	Δī	ΔP	Dry	Wet	Vol-
Power	quency	age	Load	Bff.	Weight	ght	Volume	Flow	Air	F.	3	H20	н ₂ о	Weight	Weight	c see
AUL	HZ	2	XX	RP	2	2	1	E S	5		E de	7	PS1	97	27	II
14.0	1200	20	108.3	99.2	2434	1	136.0	9080	30.6	1.5	1	,	,	1820	3160	44.7
14.0	1200	150	162.9	8.86	4450	ı	256.0	12690	32.9	1.0	•	1	1	4090	7180	103.0
14.0	1800	20	145.7	0.66	1670	1762	126.0	Nat. Cc	Convection	ion	22.5	19.9	6.5	1820	3160	44.7
14.0	1800	150	208.2	98.5	4930	ı	296.0	23400	22.8	1.5	,	,	ı	4720	8150	116.0
14.0	2500		149.5	6.86	168	810	32.0	ı	,	,	16.8	33.8	8.0	794	1470	21.0
14.0	2500	20	190.4	98.7	1670	1760	126.0	Nat. Cc	Convection		22.5	26.3	6.5	1820	3160	44.7
14.0	2500	100	231.7	98.4	4870	ı	345.0	18170	32.7	1.5	1	1	,	3100	5340	76.0
14.0	2500	150	275.2	98.1	7300	ı	519.0	27350	25.9	1.5	1	,	1	4720	8150	116.0
14.0	2500	200	322.3	95.8	6570	ı	391.0	3120	26.5	1.0	,	ı	ı	5350	9150	132.0
21.0	009	-	87.6	99.5	1170	1230	480.0	1	1	1	21.0	15.8	6.5	1190	2200	31.0
21.0	009	100	137.9	99.4	3280	ı	196.0	15600	22.7	1.5	ı	ı	1	3100	5340	76.0
21.0	909	200	186.0	99.1	5940	ı	338.0	15230	31.4	9.0	ı	,	ı	5350	9150	132.0
21.0	1800	-	164.0	99.2	1170	1230	48.0	1	1	<u> </u>	21.0	29.6	6.5	1190	2200	31.0
21.0	1800	100	233.1	98.9	4870	1	345.0	18170	32.9	1.5	,	1	1	3100	5340	76.0
21.0	1800	200	299.2	98.6	6570	ı	391.0	31200	24.6	1.0	ı	ı	ı	5350	9150	132.0
30.0	200	-	108.5		1890	,	74.3	14000	20.0	1.0	1	ı	1	1710	2940	42.0
30.0	200	20	155.2	99.5	1670	1760	126.0	Nat. Co	Convection		22.5	22.7	6.5	1820	3160	44.7
30.0	200	100	160.0	99.5	4870	ı	345.0	18170	22.7	1.5	ı	ı	ı	3100	5340	76.0
30.0	200	150	179.8	99.4	4920	1	296.0	23400	19.7	1.5	<u> </u>	1	 I	4720	8150	116.0
30.0	200	200	200.9	99.3	5940	ı	338.0	15230	33.8		1	ı	ı	5350	9150	132.0
30.0	009	20	172.4	9	1670	1760	126.0		Convection	_	22.5	25.5	6.5	1820	3160	44.7
30.0	009	150	200.6	99.3	4930	ı	296.0	\sim	22.0				1	4720	8150	116.0
30.0	1200	20	222.0	99.3	1672	1760	126.0	Nat. C	Convection		22.5	33.4	6.5	1820	3160	44.7
30.0	1200	150	257.9	99.2	7300		519.0	19250	34.3		,	ı	,	4720	8150	116.0
30.0	1800	20		0.66	1670	1760	126.0	Nat. Co	Convection		22.5	44.3	6.5	1820	3160	44.7
30.0	1800	150	344.3	98.9	7300	ı	519.0	27250	32.4	1.5	,	1	1	4720	8150	116.0
30.0	2500		321.0	6.86	1680	1760	9.89	ı	1	1	36.0	33.8	8.0	1710	2940	42.0
30.0	2500		375.0	8.86	1670	1760	126.0	Nat. Cc	Convection		31.5	41.0	19.5	1820	3160	44.7
30.0	2500	100	434.0	98.6	7370	ı	491.0	41250	27.0	2.5	1	1	1	3100	5340	76.0
0.	2500	150	467.4	98.5	7800	1	558.0	40880	29.3	1.5	,	1	1	4720	8150	116.0
30.0	2500	200	485.0	98.4	9730	-	688.0	54500	22.8	0.1	-	1	,	2960	10240	145.0

TABLE 15
INVERTER-FED RECTIFIER DESIGN POINTS

Inverter-fed rectifier:		
$P_1 = 0.5MW$	$f_1 = 5kHz$	$V_1 = 40kVdc$
$P_2 = 7MW$	$f_2 = 10kHz$	$V_2 = 80 \text{kVdc}$
$P_3 = 14MW$	$f_3 = 15kHz$	$V_3 = 120 kV dc$
$P_4 = 21MW$	$f_A = 20 \text{kHz}$	$V_A = 160 \text{kVdc}$
$P_5 = 30MW$	$f_5 = 25kHz$	$V_5 = 200 \text{kVdc}$

The numbers above shall be interpreted as output power (P), input frequency (f), and output voltage (V).

			RECTIF	ER DESIG	POINTS			
P	£	v	P	f	v	P	f	٧
1	1	1 2	2 2	4	3 5	4	2	5 1
1	1	3	3	1	1	4	4	3
1	1	4 5	3 3	1 1	2 3	5	4 1	5 1
1	2	2	3	1	4	5	1	2
1	2 3	4 2	3	1 2	5 2	5	1 1	3 4
1	3	4	3	2	4	5	1	5
1	4	2 4	3 3	3 3	2 4	5 5	2 2	2 4
1	5	1	3	4	2	5	3	2
1	5 5	2 3	3 3	4 5	4	5 5	3 4	4 2
1	5	4	3	5	2	5	4	4
2	5 2	5 1	3 3	5 5	3 4	5 5	5 5	1 2
2	2	3	3	5	5	5	5	3
2 2	2 4	5 1	4 4	2 2	1	5 5	5 5	4 5

4.1.3 Component Selection

The inverter fed rectifiers were selected from the group of manufacturers researched in Phase I. The prime parameters considered were P.I.V., speed of recovery and forward current capability. The devices selected were manufactured by International Rectifier of El Segundo, Cal. The types and ratings are as shown in Table 16.

TABLE 16
MANUFACTURER'S RECTIFIER RATINGS

Rectifier	I _F (AV) at	Max. T _C (^Q C)	PlV	Max. ^t rr (μs)
12FL100505	12A	100°	1000V	0.5
70HFL100505	70A	75°	1000V	0.5
251ULR100515	250A	105°	1000V	1.5
401PDL80515	400A	97°	800V	1.5

4.1.4 Design

This concept resulted in five basic modules, each rated at the same voltage, 40 kV, but at different current levels. Figure 23 is a chart showing the arrangement of the modules to obtain the various output voltage and power levels. Late in the design phase, the rectifier used in module "C" was dropped from IR's line. It was then necessary to replace this rectifier with the type used in module "D". This reduced the number of different modules to four. Figure 24 is a chart showing the minimum-maximum operating levels for each device and the minimum-maximum forward voltage drops to be expected at 25°C junction temperature and 175°C junction temperature. These forward drops were used in calculating the forward power loss for the modules. Figure 25 is a schematic showing the basic arrangement for one 40 kV module. Each leg of the full wave bridge contains 125 rectifiers with resistor and capacitor compensation. Each rectifier is rated at 1000 V P.I.V. Therefore, ideally the actual operating P.I.V. that each rectifier sees is 500 V.

4.1.4.1 Series Compensation

Ideally, each of the 125 rectifiers in the string would see a P.I.V. of 500 V if they all had identical characteristics, that is, identical reverse recovery time and identical reverse leakage current. Since this is not the case, compensation is required across each rectifier to assure a voltage division with a +20 percent margin.

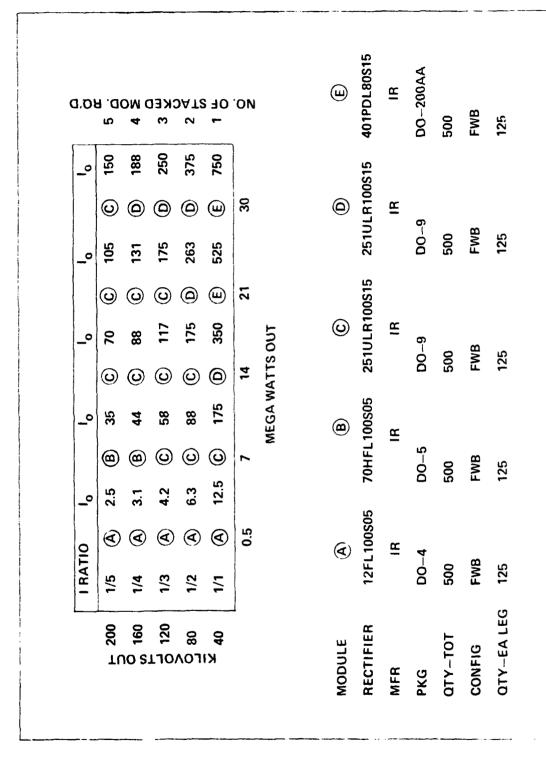


Figure 23 - Inverter-Fed Rectifiers Module Descriptions

									<u> </u>	E _F (PK)V	
RECTIFIER	USED IN MOD	i (PK) A MAX MIN	A N	I (AV) A MAX MIN	A N	l (rm MAX	I (rms) A MAX MIN	$T_j = 25^{\circ} C$ MAX MIN	50 C MIN	$T_j = 175^0 C$ MAX MIN	175 ⁰ C MIN
12FL 100 S05	4	12.5	2.5	6.25	1.25	89.	8.	1.4	1.3	1.2	1.0 (150 ⁰)
70HFL100S05	ω.	4	35	22	17.5	31	25.	1.2	7	1.3	1.25 (125 ⁰)
25IULR100S15	ပ	175	28	87.5	59	124	41	£.	1.1	1.2	6:0
25IULR100S15	Q	525	188	263	94	371	133	4.1	1.2	4.1	<u>-</u>
40IPDL80S15	ш	750	750	375	375	530	530	5:1	1.5	9.1	9.
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Figure 24 - Rectifier Operating Characteristics

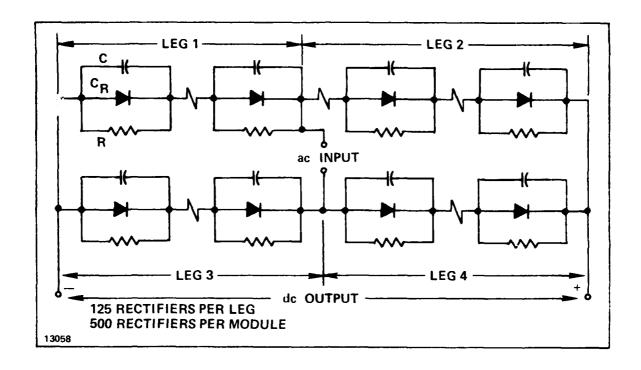


Figure 25 - Typical 40 kV Module

4.1.4.1.0 Recovery Compensation

The recovery time of a rectifier is a characteristic of the particular device and is dependent on certain operating conditions, namely, the junction temperature, the forward conducting current, I_{FM} , prior to commutation and the rate of fall of conducting forward current, A/ μ sec. Curves relating these parameters to the maximum recovered charge, Qmax, in microcoulombs are generally given on the manufacturers' data sheets for the particular device. The generally accepted method of equalizing the voltage division during recovery of a string of rectifiers is to put a capacitor across each device to minimize the effect of unequal stored charge. The maximum voltage difference that will appear across a device is then Δ Vmax = Δ Qmax/C. Worst case junction temperatures, forward currents, IFM, and rate of fall of forward current, A/ μ sec, were used to determine the capacitor values. Capacitor C was chosen to limit Δ Vmax to +20 percent.

For example, consider the rectifier type 12FL100S05 used on the A module illustrated in Figure 26. At a load current I_{DC} of 12.5A in the worst case, the average current per rectifier is $I_{DC}/2$ = 6.25A and I_{FM} = (π)(6.25A) = 19.6A. The current rate of fall di/dt = $6I_{FM}/T$, a relationship which was derived graphically during the design. At

25 kHz T = 1/f = 40 μ sec and, thus, di/dt $\approx 3A/\mu$ sec. Using the IR data sheet for this device gives a worst case recovered charge $\Delta Q = 600$ nanocoulombs. Allowing a maximum 120 volts variation in voltage division determines the compensating capacitance $C = \Delta Q/\Delta V = 600 \times 10^{-9}/120 = 0.005 \ \mu F$ as indicated in the circuit diagram on the right-hand-side of Figure 26.

4.1.4.1.1 Leakage Current Compensation

Since all rectifiers have some reverse resistance, they all will have some reverse current with an applied reverse voltage. This resistance or current is a characteristic of a particular device and is temperature sensitive. The manufacturer generally specifies the maximum leakage current at the rated PIV and maximum junction temperature. Figure 26 is a plot of this characteristic for one particular device used.

The equation
$$RS = \frac{nsEp - Em}{(ns+1) \Delta IR}$$

can be solved for the shunting resistor value required to compensate for this leakage current,

where: ns = number of series rectifiers

Ep = maximum voltage desired across a rectifier

Em = total reverse voltage applied to rectifier string

 ΔIR = possible difference in leakage current

Ep was chosen to be +20 percent of Em/ns

ΔIR was taken as 75 percent of IR at the maximum junction temperature

For example, consider the A module illustrated in Figure 26 and determine the appropriate shunting resistor value R_S . The total reverse voltage Em is given by (40 kV) (1.57) ≈ 63 kV and the maximum voltage across an individual rectifier is given by $E_p = (1.2) (63000)/125 \approx 603$ volts. The value of Δ IR at the maximum junction temperature of 150°C is found from the PK IR at 500 V line of Figure 26 to be (0.75) (3.8 mA) = 2.9 mA. The above equation for RS gives

RS =
$$\frac{(125)(603) - 63 \times 10^3}{(125-1)(2.9 \times 10^{-3})}$$
 = 34 x 10³ ohms

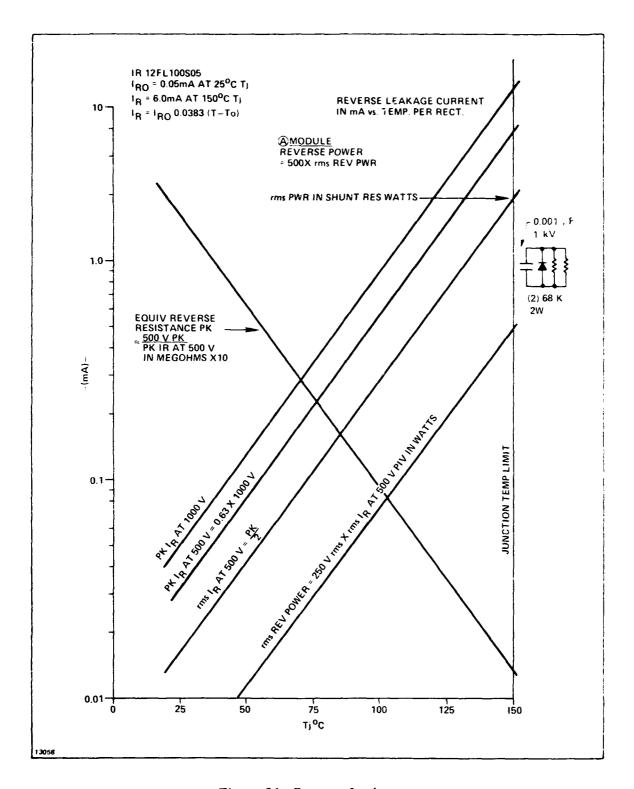


Figure 26 - Reverse Leakage

as shown in the compensation circuit diagram given on the right-hand-side of Figure 26. A pair of 68 k resistors are shown connected in parallel to illustrate the use of standard commonly available components.

4.1.5 Power Losses

The total loss for each rectifier consists of the forward conducting loss plus the reverse recovery and the reverse leakage loss. The reverse recovery loss is frequency dependent and linear. The forward loss is the product of the forward current and voltage drop and relatively independent of frequency. In addition to the rectifier losses, an additional loss occurs in each shunting resistor. Therefore, the total loss per 40 kV module is the sum of the losses for each rectifier and its shunt resistor or 500 x (rectifiers and resistor loss).

4.1.5.1 Rectifier Losses

The rectifier loss consists of the forward loss plus the reverse recovery loss and the reverse leakage loss. The reverse recovery loss is also related to frequency.

Figure 27 is a graph of the forward loss for each rectifier and each module at all power points and voltage points. The forward loss can be considered constant over the 5 to 25 kHz frequency range.

Figure 28 is a graph of the reverse recovery loss for each rectifier diode at all output voltage level points at 5 kHz. These losses increase with frequency as shown by the frequency multiplier. They increase by the factors 2,3,4,5 at 10,15,20,25 kHz. It can be seen from the curve that the recovery loss increases with the forward current level also.

Figure 26 shows the losses attributed to reverse leakage current for a rectifier diode at various junction temperatures.

4.1.5.2 Shunt Resistor Losses

The shunt resistor values were calculated to compensate for the reverse leakage current of the diodes at the maximum junction temperature. Therefore, this is a fixed loss at the 40 kV module level and is independent of frequency and temperature.

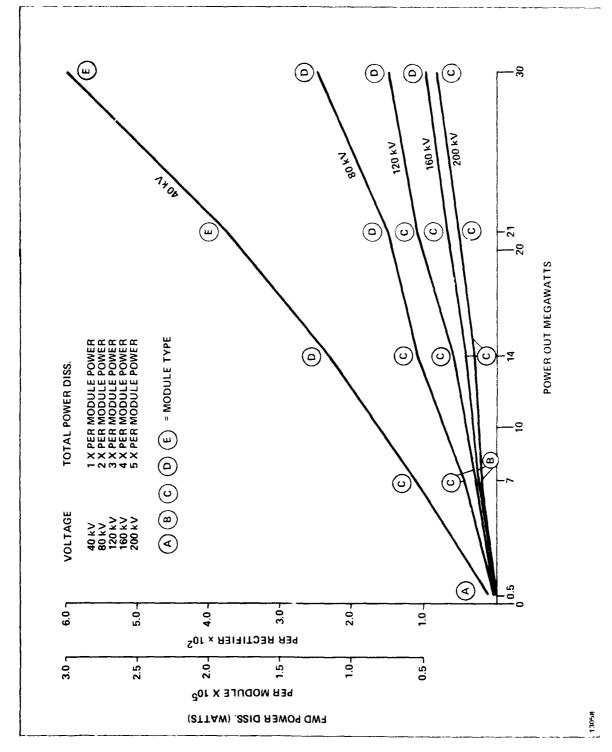


Figure 27 - Forward Power Dissipation For Inverter-Fed Rectifiers

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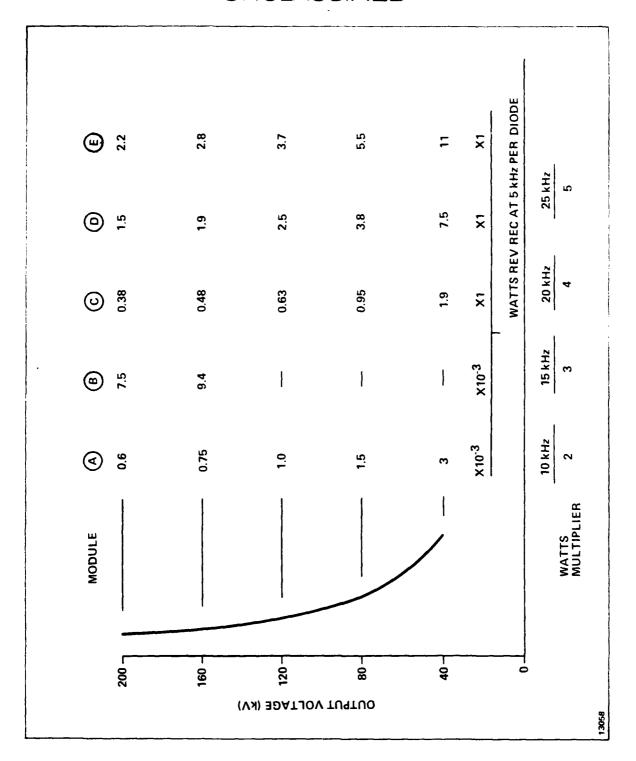


Figure 28 - Reverse Recovery Losses for Inverter-Fed Rectifier Modules
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4.1.6 Total Losses

As previously mentioned, the total loss for a 40 kV module is 500 times (the sum of the forward conducting loss of the diode plus the reverse leakage loss, plus the recovery loss, plus the shunt resistor loss) at a given load current level and frequency level.

It is these values that were used in the 60 design points for the mechanical design.

4.2 Mechanical Design

Sixty design points were evaluated for both minimum weight and minimum volume designs. Ambient conditions were assumed to be 20°C and a pressure range of 20.58 to 29.92 in. of mercury, corresponding to an altitude range from sea level to 10,000 ft. Cooling media included forced air, natural convection, water and oil. Conventional components, heatsinks and accessories were used. No allowance was made for electrical or mechanical interfaces such as high voltage bushings, etc. between subsystems. It was determined that such interfaces would vary so widely with application and choice of subsystems that no truly representative approach could be applied to this aspect of isolated subsystem design.

The minimum weight designs are air insulated with air-cooling, except for four design points which require water cooling. The minimum volume designs are nearly all adiabatic with the exception of two design points for which oil flow may be advisable because of marginally high temperature excursion in the oil.

The results for the inverter-fed rectifier designs are presented in Table 17. The densities are typically 20 lb/ft³ for the minimum weight designs above 0.5 MW and approximately 90 lb/ft³ for the minimum volume designs. In the case of the four water-cooled minimum weight designs, the density drops to about 11 lb/ft³. Densities for the 0.5 MW designs are in the range of 11 to 17 lb/ft³ for minimum weight and 81 to 85 lb/ft³ for minimum volume.

5. INVERTER PHASE II

One hundred sixteen specific design points were evaluated. Input voltage varied from I kV to 28 kV, output power from 500 kW to 30 MW at conversion frequencies from 5 kHz to 25 kHz and output voltages from 40 kV to 200 kV.

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Practical designs appear to be limited to 1 kV input voltage, 5 to 10 kHz conversion frequency and 500 kW output power. These limitations are dictated by breakdown voltage of the high speed solid state switches (Silicon controlled rectifiers). Series connection of more than four of these devices will not produce reliable operation. Consequently, because of the 1 kV operation, the output power is limited by the current-handling capability of the SCR, approximately 2000 A peak which limits the maximum output power to 500 kW maximum. Component values were calculated for all 111 design points and evaluated on the basis that in the future a more suitable, fast high voltage solid state switch will be available. All other components appear to be within the capabilities of today's technology.

5.1 Electrical Design

5.1.1 Inverter Design

The design analyzed is a parallel resonant bridge inverter described in Subsection 2.3 of this report. The inverter consists of two resonant inverters that are started with their voltages in phase. A load is connected between the two. Since the instantaneous voltage at the output of each inverter is identical, no initial voltage is present across the load. Changing the phase of one inverter relative to the other will produce a voltage difference across the load. Usually the maximum phase shift allowed is 144 degrees because of the stability problems stated in Subsection 2.3.1.

5.1.2 Component Ground Rules

During the analysis, the following ground rules were adhered to.

- No greater than 2,000 A peak will flow in any branch of the circuit.
 This limit was chosen because of SCR current rating.
- 2) Capacitor current will be limited to 175 A rms because of capacitor bushing limitations.
- 3) Maximum peak voltage per SCR is limited to 700 V. Based on the best available SCR for high frequency inverter application and allowing for reasonable voltage derating. (Specification limit 1000 V for a fast SCR.)
- 4) 4000 V maximum stress per saturable reactor.

5.1.3 Design Points

Capacitor values, inductor values, transformer parameters, saturable reactors, were calculated for all 116 points.

The solid state switches (SCRs) limit the practical input line voltage to 1 kV. High speed SCRs are available that can handle 1 kV each. Reasonable derating to 700 V is advisable for a reliable design. During inverter operation, the peak voltage across the switch will approach two and one half times the line voltage. Therefore ((1 kV +10 percent) x 2.5) = 2.75 kV. Four SCRs in series will be required. The next available voltage is 7 kV which would require 28 SCRs in series. Reliable commutation of 28 SCRs at the conversion frequency of 5 kHz minimum is not obtainable with today's technology. Therefore, the usable input voltage is limited to 1 kV. Practical current handling capability of high speed SCRs is approximately 2000 A peak. The combination of 1000 V, 2000 A and the circuit operating Q limit the output power to 500 kW at 5 and 15 kHz conversion frequencies. At a conversion frequency of 25 kHz, the current must be dropped to approximately 1000 A because of the per cycle switching losses. Therefore, the maximum output power is 250 kW at 25 kHz conversion frequency.

5.1.4 Typical 0.5 MW 1 kV Module

A typical 0.5 MW 1 kV module will operate as described in Subsection 2.3.1 of this report. The schematic is as shown in Figure 5 except that each SCR and its corresponding snubber network will require four SCRs and snubbers connected in series and a resistor in parallel with each SCR. Also, the commutating capacitors will require four each capacitors connected in parallel to stay within the rms current rating of the capacitor bushings. The count of all components remains the same, one diode/SCR string, one saturable reactor/string, etc. Efficiency of the inverters at all frequencies varies from 85 to 90 percent, 25 kHz being the least efficient and 10 kHz being the best, but only slightly better than 5 kHz. To obtain higher power output at 1 kV input voltage, the study paralleled the outputs of an appropriate number of 500 kW modules to produce the required output power (e.g., 14 required for 7 MW out).

Selection of the SCRs will follow the criteria set forth in paragraph 5.1.3. Capacitive and resistive compensation across the series-connected SCRs are designed in the same manner as the diode string discussed in paragraph 4.1.4.1. That is, capacitive

compensation is required for reverse recovery charge differences and resistive compensation is added for differences in leakage.

The bulk of the losses (72 percent) are distributed equally between the SCRs and the series resonant inductors. The output transformer and control circuitry account for 11 percent and 4 percent respectively. The remaining 13 percent are distributed equally among the saturable reactors, SCR shunt diodes, snubber networks and series resonant capacitors.

5.2 Mechanical Designs

Thirty-three design points were evaluated for minimum weight design. The same 33 design points were then evaluated for a minimum volume design. A starting temperature of 20°C and pressure from 20.58 to 29.92 in. of mercury were used. Cooling media were air, water, oil. Conventional components and heat sinks and accessories were utilized. No allowance was made for electrical or mechanical interfaces with other subsystems (e.g., high voltage bushings, connectors, air ducts, etc.).

The results show that the minimum weight design is air insulated with air and water cooling and voltage isolation provided only at the mounting surface. Minimum volume design was produced with the electronics enclosed in a tank of oil and water cooling provided.

Each of the major components were cooled as follows:

	Type De	sign
· · · · · · · · · · · · · · · · · · ·	Min Weight	Min Volume
SCRs	Water	Oil
Diodes	Air	Oil
Output Transformer	Adiabatic	Adiabatic
Linear Reactor	Adiabatic	Adiabatic
Saturable Reactor	Water	Water
All Resistors	Air	Oil
All Capacitors	Adiabatic	Adiabatic
Control Circuitry	Air	Oil

The saturable reactors, because of their small size and high heat density, require water cooling in both the minimum weight and minimum volume design.

Transformer analysis at the power level being considered produced unusual results. Normally one would expect the transformer size to decrease in proportion to the square root of the increase in frequency. The factor $\sqrt{f2/f1}$ requires that a constant flux density be utilized in the core material. In the transformer designs executed, it became apparent that considerable insulation would be required. Also, due to the high currents involved, copper thickness was limited by skin effects and proximity effects. The added insulation and high current density combine to limit the minimum coil size, therefore the minimum practical core size. Since the core size is limited, the core flux density decreases with an increase in frequency as illustrated in Figure 29 invalidating the $\sqrt{f2/f1}$ relationship. Figures 30 and 31 illustrate the weight and volume of the transformer versus frequency. A point of diminishing return is reached at approximately 10 kHz. Also, notice that as the voltage increases, the weight and volume increase in an accelerated manner because the insulation is becoming an increasingly larger percentage of the coil area.

5.3 Summary Tables and Conclusions

Table 18 presents the results of the inverter study for the minimum weight and the minimum volume designs. Major points to be kept in mind when evaluating the results are that all transformers are designed to be run in oil. The minimum weight design must contain a case for the transformer and the oil. Minimum volume designs have the entire electronics immersed in oil; therefore, the transformer weight is just the coil and core.

If the input voltage, conversion frequency and output power are held constant, a transformer becomes less efficient with increased output voltage because of the poorer coupling caused by the increased insulation requirements.

As the conversion frequency increases, SCRs and their associated snubbers and saturable reactors are the major cause of increased inefficiency since their losses are on a per cycle basis. Transformer losses descrease because of the lower flux density as described earlier in this report.

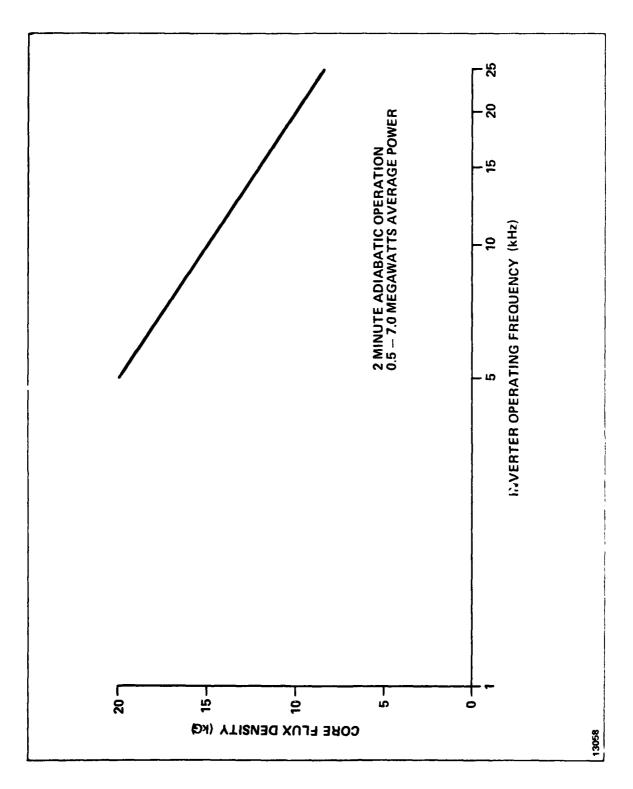


Figure 29 - Inverter Power Transformer Design Flux Density

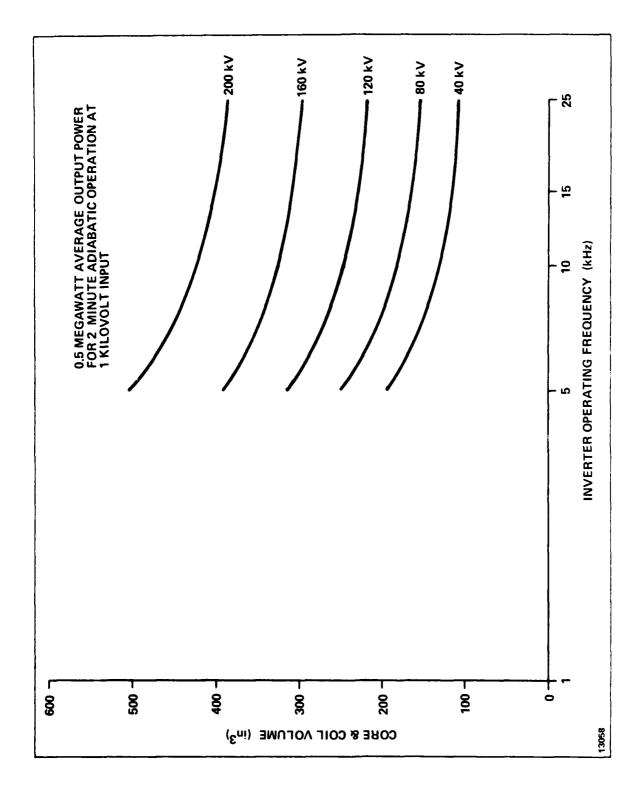


Figure 30 - Inverter Power Transformer Core and Coil Volume Versus Output Voltage and Operating Frequency

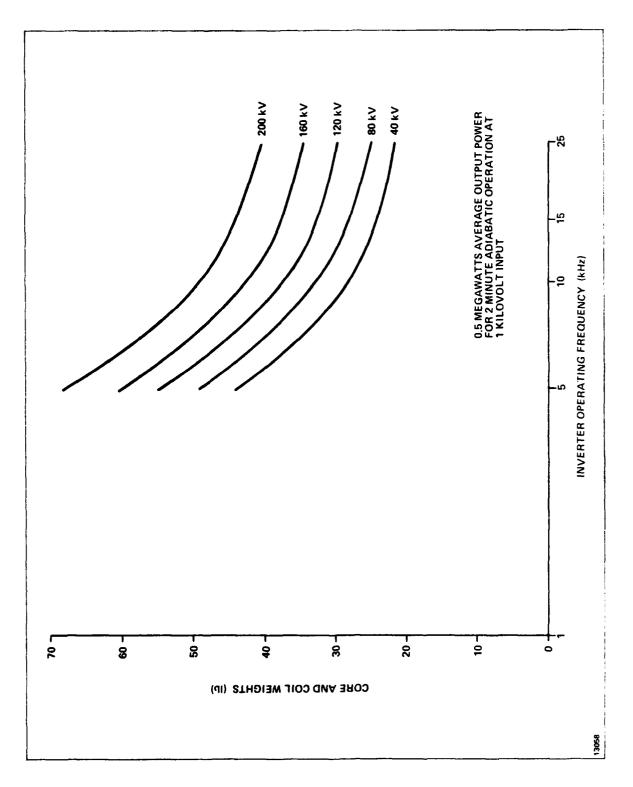


Figure 31 - Inverter Power Transformer Core and Coil Weight Versus Output Voltage and Operating Frequency

Since it became apparent during in this study that it was not possible to use SCRs in this configuration at input voltages greater than 1000 V, it was agreed that in lieu of providing all designs at higher voltages, we would perform additional analysis at 1000 V, 500,000 W and 10 kHz. This information is also presented in Table 18.

A series resonant bridge inverter can be built with presently available hardware at a conversion frequency of 5 to 10 kHz and 1 kVdc input voltage to provide an output of 500 kW at 40 kV to 200 kVdc.

6. PULSE FORMING NETWORK PHASE II

Sixty-five design points were evaluated for both minimum weight and minimum volume resulting in a total of 130 point designs. These designs followed closely the preliminary design approach except that no inverter charging circuits were employed.

6.1 Electrical Design Approach

A certain commonality was determined which allowed the selection of groups of components such as PFLs, charging chokes and diode assemblies. These groups were then used as building blocks for the required design points. Present state-of-the-art components were used except for the charging chokes which were specially designed during the study.

6.1.1 Pulse Forming Lines

The PFL configurations each used groups of 12 capacitors arranged with thyratrons according to Figure 10, depending on pulse duration. Capacitor value and energy storage were used to describe five basic types of PFL from which each point design could be constructed. These PFL types are described in Table 19.

Because of the reduced operating burst duration (120 sec) allowed for the Phase II designs, the capacitor energy density has been set at a nominal 70 J/lb. However, as indicated in Table 19, the actual densities vary with the unit capacitance chosen. This results from effects of case margins used in scaling a 60 J/lb, 0.84 μ F capacitor of known dimensions.⁽⁵⁾ A dissipation factor of 0.5 percent was used to calculate losses in the PFL capacitors.

⁽⁵⁾ From Reference 2, p. 8

TABLE 18 VERTER DESIGN RESULTS

TOTAL INTERNAL	STATE OF THE STATE	Det ion Trace	Section 1	and ton	L	200	TO VET	5				Air Plos		Byo FLON	5 8		No. PLON	
ge Frequency Voltage Min Mt. Min Vol. Min Mt.	Conversion Output Frequency Voltage Min Wt. Min Vol. Min Wt.	Output Voltage Min Wt. Min Vol. Min Wt.	Min Wt. Min Vol. Min Wt.	Min yol. Min Wt.	Min Wt.		Min Vol.		Min Wt. Min Vol.	Efficiency		10. H.O.	(B)	হ	(CO) QP (PS1)	M	04 (دو)	क्षेत्र के
20.6 781	40 23.2 20.6 781	23.2 20.6 781	20.6 781	20.6 781	182	1_	721	(dt)	1.340	89.8	56.9	828	2.5	32.9	2	1 3	12.9	-
80 23.8	80 23.8 21.2	23.0 21.2	21.2		908		727	848	1,360	69.0	62.1	828	2.5	L_ l	8	6.5	12.9	-
1 5 120 24.6 21.8 829	120 24.6 21.8	24.6 21.8	21.8	_	629		733	988	1, 390	88.9	62.5	828	2.5	32.9	g	6.5	14.9	-
1 5 160 25.2 22.4 849	160 25.2 22.4	25.2 22.4	22.4		698		739	938	1,410	88.8	63.1	828	2.5	32.9	2	6	6.71	4
1 5 200 25.9 23.0 891	200 25.9 23.0	25.9 23.0	23.0	_	1691		747	1,040	1,440	68.7	63.6	628	2.5	32.9	g	\$	12.9	-
1 10 40 18,1 16,1 603	40 18.1 16.1	19.1 16.1	16.1	_	603		584	635	1,050	89.9	56.4	1,010	4.0	23.3	Ξ	0.5	7.6	7
1 10 60 18.9 16.8 626	80 18.9 16.8	18.9 16.8	16.8	_	929		589	676	1,090	89.8	56.7	1,010	•.0	3.3	=	9	19.7	-
1 10 120 19.8 17.6 650	120 19.8 17.6	19.8 17.6	17.6	_	650	1	594	121	1,130	8.68	57.1	1,010	•.0	3.3	2	5.0	19.7	7
1 10 160 21.1 18.8 678	160 21.1 18.8	21.1 18.8	18.8	_	678		599	791	1,200	69.7	57.5	1,010	4.0	23.3	3	5	7.67	-
1 10 200 21.6 19.2 706	200 21.6 19.2	21.6 19.2	19.2	-	902		909	969	1,210	89.6	58.0	010'1	4.0	23.3	=	0.5	7.51	-
1 15 120 15.9 14.2 526	120 15.9 14.2	15.9 14.2	14.2	_	526		523	586	915	89.9	56.0	1,030	6.0	17.4	22	3.	26.7	7
1 25 120 25.0 22.2 713	120 25.0 22.2	25.0 22.2	22.2	_	113		757	817	1,400	85.2	8.98	1,770	Ξ	13.5	7	-	97.9	
7 10 40 356 292 11,580 1	40 356 292 11,580	356 292 11,580	292 11,580	11,580			11,240	11,970	21,300	90.7	71.5	13,770	72	60.0	02	۰	¥.4	4.5
7 10 120 356 292 11,630 1	120 356 292 11,630	356 292 11,630	292 11,630	11,630	-+		11,290	12,180	21,350	9.06	722	13,770	*	6.0	20	٥	36.4	1.5
7 10 200 356 292 11,690 1	200 356 292 11,690	356 292 11,690	292 11,690	11, 690			11, 350	12,530	21,410	90.6	729	13,770	74	40.9	2	٥		5:5
1 10 200 302 257 9,880	200 302 257 9,880	302 257 9,880	257 9,880	9,880	 ↓		8,320	12,170	16, 180	9.68	912	14, 100	56	30.7	=	-	7.61	7
1 5 40 649 541 21,870 1	40 649 541 21,870	649 541 21,870	541 21,870	21,870	+		19,580	22,650	35,220	89.8	1590	23,180	70	32.9	2	=	6.71	-
1 5 80 668 557 22,510 19	668 557 22,510	668 557 22,510	557 22,510	22,510	+	- 51	19,740	23,740	35,870	0.68	1740	23,180	20	32.9	30	4	\$ 71	1
1 5 120 688 574 23,210 19	688 574 23,210	688 574 23,210	574 23,210	23, 210	- +	=1	016'61	25,090	36, 560	6.98	1750	23,180	2	32.9	90	7	6.77	-
1 5 160 704 589 23,770 2	704 589 23,770	704 589 23,770	589 23,770	23,770		~!	20,070	26, 260	37,160	88.8	1770	23,180	2	32.9	8	=	6.24	
1 5 200 725 605 24,950	725 605 24,950	725 605 24,950	605 24,950	24,950	-+		20, 290	29,060	37,620	88.7	1780	23,180	2	9.25	2	=	6.71	7
1 15 120 446 372 14,730	120 446 372 14,730	446 372 14,730	372 14,730	14,730	- ;		14, 200	16,410	24,080	6.68	1570	28,870	166	17.4	22	=	7.97	
1 25 120 700 584 19,960 2	120 700 584 19,960	700 584 19,960	584 19,960	19,960	-+	(4)	20,560	22,880	36,980	85.2	2430	69,610	392	13.5	#.	87	37.9	
7 10 40 1070 876 34,740	40 1070 876 34,740	1070 876 34,740	876 34,740	34,740	\rightarrow		33,720	35,910	63,880	90.7	2150	41,320	27	40.9	21	27	 	5.7
7 10 120 1070 876 34,900	120 1070 876 34,900	1070 876 34,900	876 34,900	34,900	\rightarrow		33,870	36,540	64,040	9.06	21.70	41,320	7.7	6.0	70	27	9	\$1.5
7 10 200 1070 876 35,080 3	200 1070 876 35,080	1070 876 35,080	876 35,080	35,080			34,050	37,600	64,220	9.06	2190	41,320	7.5	6:3	07:		4	- T
1 5 40 1390 1139 46,860 4	40 1390 1139 46,860	1390 1139 46,860	1139 46,860	46,860	-	₹,	41,600	48,540	74,110	8.68	34.20	69,680	150	6.4	8,	30	, , , , , , , , , , , , , , , , , , ,	~
1 5 80 1431 1172 48,240 4	80 1431 1172 48,240	1431 1172 48,240	1172 48, 240	48,240		=	41,940	50,880	75, 490	0.68	3720	49,680	150	34.9	œ:	0 7	, s	1
1 5 120 1474 1207 49,740	1474 1207 49,740	1474 1207 49,740	1207 49,740	49,740		-	42,290	53,760	76,940	6.88	3750	49,680	150	32.9	30	9	5.7	
1 5 160 1509 1240 50,940	1509 1240	1509 1240	1240	1	50,940		42, 630	56, 280	78,200	88.8	3790	49,680	150		2	<u>.</u>	6 7	
1 5 - 5 - 200 1553 1273 53,460	1553 1273 53,460	1553 1273 53,460	1273 53,460	53,460			43,100	62,280	79,590	88.7	0781	989 '€ \$	9.	3	ž	<u>.</u>	,	-,
1 15 - 120 + 956 784 . 31,560 3	956 784 31,560	956 784 31,560	784 31,560	31,560			30,170	15, 160	50,683	7.68	3360	41,860	36.		77	<u> </u>	r	~
25 120 1566 1230 42,780 4	1566 1236 42,780	1566 1236 42,780	1236 42,780	42,780		4	41,670	49.020	77,420	85.7	5,410	106,440	940	\$	π:	3	3.	

TABLE 19
PFL CLASSIFICATION

PFL Type	Capacitor Value-µF	Number of Capacitors	Energy Stored in PFL-kJ	Capacitor Density J/lb
а	0.25	12	2.4	58.5
b	0.33	12	3.13	62
С	0.45	12	4.32	66
đ	0.50	12	4.80	67
e	0.66	12	6.25	69

Inductance values were calculated for each combination of PFL type and pulse duration. Using the formula for single-layer solenoids the inductors were designed and the losses were calculated. Losses were based on the AC resistance during the rise and fall of the pulse and the DC resistance during the flat portion of the pulse. (6)

6.1.2 End-of-Line Clippers

The end-of-line clippers have been sized to withstand the reverse pulse current of a dead short circuit and the average current and power due to a steady 25 percent undermatch at the PFN load. The effect of mismatch has been illustrated in Figures 8 and 9. Approximately 2 percent of the power incident on the load would be reflected in this case. Diode current rating was determined as described earlier in Subsection 2.4.3. For the most part, clippers are made up of 40 stud-type diodes (Westinghouse R500-15) in series. A few designs required the additional current and thermal capabilities of the puck-type devices (Westinghouse R620) which have been used in stacks of 20. In general, the 5 and 10 sec designs required two clipper stacks per module (see Figure 10) and the longer pulse durations required one stack per module.

⁽⁶⁾ Glasoe, G.N. and Lebacqz, J.V., eds., Pulse Generators, McGraw-Hill, New York (1948), p. 214.

6.1.3 Charging Circuits

Wherever possible sequential, four-module charging is used to smooth out the charging current and keep the charging chokes at reasonable sizes. Those design points which have less than four thyratrons or have a number of thyratrons not evenly divisible by four are not suitable for this approach. For example, each of the 0.5 MW designs utilizes only one or two thyratrons and therefore has a single charging module. Also, design points 17 and 31 were found to require nine and 18 thyratrons, respectively, so three charging modules were used in these cases.

The basic charging module (or submodule) services two thyratrons and their associated PFLs. Larger charging modules (those servicing two, three or four pairs of thyratrons) have multiple charging chokes in parallel in direct proportion to the increased PFL capacitance to keep the charging time constant. Thus, each PFL type (Table 19) has a specific charging inductance specified for it for each of the ten possible pulse repetition frequencies (PRFs).

In the four-module sequential charging there is an overlap such that each charge takes about one-third of the available time. An allowance of 200 μ sec is added for thyratron recovery prior to reapplication of charging voltage after a pulse. The charging period in milliseconds for which each choke is designed is related to PRF by

$$T_{charge} = 1/3 \frac{(1000)}{PRF} - 0.2$$

A total of 13 separate charging chokes were specified and designed. Their values and the numbers of chokes used for each design point are summarized in Table 20.

Also part of the charging module are the blocking diodes and command SCRs. Each blocking diode is rated for 1.5 times the PIV of 40 kV. Each stack is comprised of 20 diodes each rated 3 kV. In Table 20 the diodes are indicated as "S" for stud-type (Westinghouse R600-20) and "P" for puck-type (Westinghouse R620-30). Similarly, the command SCR stacks are rated for twice the normal hold-off voltage of 20 kV and are made up of 20 diodes each rated for 2 kV. In Table 20 the SCRs are indicated as "S" for stud-type (Westinghouse T700-35) and "P" for puck-type (Westinghouse T750-55). Compensating RC networks are included in each diode and SCR stack.

A snubber circuit is included in each charging module to divert high frequency spikes which might otherwise occur between the charging SCR and the input to the charging choke.

TABLE 20 CHARGING CIRCUIT DESIGNS

		Charging	Choke			Blocking	con
Design Point	Average Power (MW)	Inductance Per Choke (mH)	Weight Per Choke (1b)	Qty. Per Module	Qty. of Modules	Diodes Stacks Per Module	SCR Stacks Per Module
1-5	0.5	276	90	1	1	1 - S	1 - S
6-10	7	15.9	63	1 1	1 4	1-S	1 - S
11-15	7	33.8	88		4	1-s	1 - S
16	7	116	80	1 3 2 2	3	3 - S	1-S
17	7	78	79	2		2-S	1-S
18-20	7	104	75		4	2-S	1 - S
21-25	7	140	89	2 2 3	4	2 - s	1-S
26-30	14	15.9	63	2	4	2-P	1-S
31	14	27.8	75	3	3	3-s	1-S
32-35	14	25	77	2 2	4	2-P	1-S
36-40	14	33.8	88	2	4	2-P	1-S
41-45	21	8.93	45	3	4	3-S	1-P
46-50	21	15.9	63	3 3 2	4	3 - s	1-P
51-55	21	14.6	82	2	4	2-S	1-P
56-60	30	4.97	65	2	4	2-9	I-D
61-65	30	6.85	77	2	4	2-P	2-P

6.1.4 Risetime Variations

One task of this program was to evaluate the impact on subsystem efficiency, weight and volume of varying the risetime for designs 24, 29, 44, 49 and 64 through the range of 1.5 to 6 μ sec.

The design points in question are all for a pulse duration τ of 30 $\mu\,sec$ for which the nominal risetime τ_r is determined from

$$\frac{\tau_r}{2N} = \frac{\tau}{2N} = \frac{30 \text{ } \mu \text{sec}}{2 \text{ } \times 12} = 1.25 \text{ } \mu \text{sec}$$

A sthe number of sections in each PFL (see Figure 10).

Therefore, the existing PFL configuration is adequate for the entire range of risetimes. Increase in risetime could be attained by simply allowing some additional inductance in the discharge circuit or in the anode circuit of the thyratrons.

No change would be required in the number of thyratrons since average current is the determining factor for all the points in question. Neither peak current nor di/dt would dictate a change in the number of thyratrons for this range of pulse risetime.

The principal effect of the variation in risetime would be found in the design and construction of an output pulse transformer which might be used with these PFN subsystems. The leakage inductance, load impedance and secondary voltage would combine to impact the transformer design. Apart from the transformer, which is not a subject of the present study, it can be concluded that the effect of the risetime variations mentioned above would be negligible on the PFNs as presently configured.

6.2 Mechanical Design Approach

Mechanical designs have been prepared for both minimum weight and minimum volume configurations for 65 design points. The environment included an ambient temperature of 20°C and a pressure variation from 20.58 to 29.92 in. of mercury, that is, from sea level to 10,000 ft altitude. Cooling techniques included the use of air, water, oil and heat absorption by component mass described as "adiabatic".

Conventional components, heat sinks and accessories were used. Neither electrical nor mechanical interfaces such as connectors, bushings, air ducting, etc. between subsystems were considered since such interface devices could be expected to vary widely with the particular application of individual subsystems.

Minimum weight designs utilized ambient air insulation, forced air and water cooling, and provided voltage isolation from surroundings only on the mounting base. Minimum volume designs were enclosed in oil tanks and used water cooling or the adiabatic heat absorption capability of oil, for cooling and heat transfer.

Cooling techniques used for each of the PFN components are listed in Table 21. In the minimum weight designs all the blocking diodes are air-cooled except for the 30 MW design points 61 through 65. Similarly, all the command charge SCR stacks are air-cooled except for design points 41 thorugh 65.

TABLE 21
PFN COMPONENT COOLING

T.	Cooling	Technique
Component	Min. Weight	Min. Volume
Thyratrons	Air	Oil
Pulse Capacitors	Adiabatic	Adiabatic
PFL Coils	Water	Oil
Clipper Diodes	Air	Oil
Clipper Resistors	Water	Water
Blocking Diodes	Air/Water	Oil
Command SCRs	Air/Water	Oil
Snubber Network	Air	Oil
Charging Choke	Adiabatic	Adiabatic

6.3 Results

The design data are summarized in Table 22 for minimum weight and volume. In general, the minimum volume designs result in a considerable weight penalty. The density, based on wet weight, is about 20 lb/ft³ for the minimum weight designs and increases to approximately 65 lb/ft³ for the minimum volume designs. Most of the weight increase is due to packaging in oil rather than air to achieve minimum volume.

7. CONCLUSIONS

Phases I and II of this program have resulted in preliminary and detailed designs of four power conditioning subsystems using presently available components and technology. The numbers of detailed designs are summarized in Table 23.

The inverter designs were limited by the capability of SCR switches in terms of voltage and high frequency operation.

In general, the necessity of packaging in oil to achieve minimum volume resulted in a substantial weight penalty over the minimum weight designs. Typically, a reduction in volume of 50 percent was accompanied by a weight increase by a factor of two.

Interfacing elements such as bushings, and interconnections which would be involved in any system comprised of several of the subsystems were not included because these items would vary widely from one system to another. In fact, economies in weight and volume would probably result if two or more subsystems could be packaged in a common envelope. An example of this was demonstrated by the inverter-charged PFN studied during Phase I.

TABLE 22 PFN DESIGN RESULTS

	Avg.		Rep.	Pulse	Test al	Volume		ry) Weight		et) Weight		Heat Load	ALE Play (CPM)	H ₂ O Flo	_
esign		Energy			Min. Wt.	Min. Vol.	Min. Wt.	Min. Vol.	Min. Wt.	Min. Vol.	Bff.	Total	Air Plow (CFM) el in H ₂ O, 40C ^O ΔT	eapsi, 4000AT	Mil
No.	(30/)	(EJ/P)		زعرا	(ft³)	(ft ³)	(1b)	(15)	(16)	(fp)		kW	Min, Weight	Min. Weight	Volu
1	0.5	10	50	5	39.2	30.9	842	1 • 872	857	1800	89.7	57.5	860	57	1.5
2	0.5	10	50	10	30.3	23.9	695	715	710	1430	90.6	51.9	7.30	1.22	1.3
3	0.5	10	50	20	30.3	21.9	711	732	726	1450	90.8	50.8	730	1.12	1 113
4	0.5	10	50	30	31.5	24.9	660	679	676	.410	90.8	50.8	730	1.12	1.3
5	0.5	10	50	40	32.8	25.8	675	694	692	1460	90.8	50.8	730	1.11	1.0
	ĺ			{	(ĺ	1			()			1	l
6	7	25	280	5	129	89.2	2630	2710	2770	5770	94.3		7440	18.9	i .4.6
7	7	25	280	10	129	89.2	2710	2790	2850	5850	94.6	397	7440	16.1	14.8
8	7	25	280	20	129	89.2	2560	2630	2700	5690	94.7	388	7440	15.3	. 14.8
9	7	25	280	30	135	92.8	2640	2710	2780	5910	94.7	388	7440	15.3	14.8
10	' '	25	280	40	140	96.4	2720	2800	2050	6130	94.7	388	7440	15.3	14.6
11	7	50	140	5	194	122	3930	4040	4100	8230	93.8	459	7840	19.1	4
12	7	50	140	10	180	113	3720	3820	3880	7690	94.5		7306	15.1	
13	7	50	140	20	180	113	3520	3620	3670	7480	94.6		7300	14.3	13.0
14	7	50	140	30	163	102	3220	3320	3390	6780	94.6	400	7300	14.4	8
15	7	50	140	40	170	106	3280	3380	3450	6990		400	7300	14.4	13.6
	, ,			ł			1	ļ	į)	:
16	7	75	93.3	5	291	182	5840	6010	5980	12450		482,12	6470	19.1	14.
17	7	75	93.3		221	1 18	4460	4590	4660			508.84		26.3	19.6
18	7	75	93.3		206	129	4340	4460	4480	8990		476	7310	14.7	14.
19	7	75	93.3		214	134	4460	4590	4620		93.6		7310		. 4.
20	7	75	93.3	40	222	139	4600	4730	4770	9660	93.6	478	7310	14.7	.4.
21	7 1	100	70	5	415	267	7330	7540	7520	17350	92.4	579	9313	: ! 19.1	14.
22	7	100	70	10	295	190	5880	6050	6030	1288C	93.2		7763	15.1	13.
23	1 7 1	100	70	20	290	187	5790	5960	5970	12660	91.4	496	7280	13.1	
24	1 6	100	70	30	240	154	5070	5220	5250	16720	93.4	496	7280	14.4	
25	7	100	70	40	249	160	5010	5150	5200		191.4		7286	14.4	
• /	· :	100		1		100	70.0	,,,,,	,200	10000	73.4	470	7200		
26	14 [50	280	5	277	175	5260	5400	5540	11700	94.3	847.55	14530	37.8	Ξġ.
27	14	50	280	10	277	175	5410	5570	5700		94.7	789	14530	33	24.
28	14	50	280	20	277	175	5100	5250	5380	11540	94.8	77:	14530	30.6	29.
29	14	50	280	30	288	183	5260	5420	5520	11990	94.8	772	14530	Jû.o	29.
30	14	50	280	40	299	189	5430	5590	5740	12420	94.8	771	14530	30.6	29.
				j)		:				I.	
31	14	75	186.6	5	300.72	193	6240	6420	6498	11400	94.	880	14615	1.8د	26.
32	14	75	186.6		294.94	190	5936	6100	6200	12940	94.7	790	14390	31.3	28.
33	14	75	186.6		294.94	190	5710	5870	5990	12720	94.8	768	:4390	29.3	28.
34	14	75	186.6		307	197	5840	6010	6130	13140	94.8	768	.4390	د. 29	-8-
35	14	75	186.6	40	319	205	5980	6150	6270	13570	94.8	768	14390	29.3	28
36	14	100	140	5	415	267	7780	8000	8040	17810	94.0	893.3	15390	1 38.2	28.
37	14	100	140	10	386	256	7420	7640	7740		94.7	790	14310	10.1	27.
38	14	100	140	20	386	256	7140	7340	7440	16730	94.8	774	14320	28.5	27.
39	14	100	140	30	327	2.0	6440	6620	6770	14240	94.8		14326	26.8	27.
40	14	100	140	40	339	218	6550	6740	6900	14670	94.8	776	14320	28.7	27.
	!			5	384						1				٠.
41	21	50	420		,,,,	247	6880	7070	7230	16100	94.7		19940	54.1	38.
42	21	50	420	10	384	247	7020	7220	7390	15950	95.1	1090	19940	45.9	30.
43	21	50	420	20	384	247	6530	6720	6890	15450	95.1		19940	43.5	38.
44 45	21	50 50	420	30	399	257	6820	7010	7190	16420	95.1		19940	43.4	36.
• >	21	טפ	420	40	415	267	7100	7310	7500	17100	95.2	1000	19940	43.3	38.
46	21	75	280	5	388	251	7360	7570	7790	16770	94.2	1285	20040	60.6	44.
67	21	75	260	10	368	251	7600	7810	6030	17010		1200	20040	52.3	44.
48	21	75	280	20	388	251	7130	7340	7560	16530	94.7	1170	20040	49.7	44.
49	21	75	280	30	404	262	7380	7590	7760	17180		1170	20040	49.7	44.
50	21	75	260	40	420	271	7620	7840	8090	17820	94.7	1170	20040	49.7	44.
							,								
51	21	100	210	5	415	267	7760	7980	8180	17790	94.2		20040	63.2	45.
52	21	100	210	10	415	267	7750	7970	8170	17780	94.6	1190	20040	53.4	45.
53	21	100	210	20	415	267	7420	7640	7840	17440	94.8	1140	19900	48.5	43.
54	21	100	210	30	432	278	7630	7850	8070	18080	94.9		19900	48.4	43.
55	21	100	210	40	449	289	7850	8070	8300	18710	94.9	1140	19900	48.3	43.
56	30	75	400	4	512	129	8840	9090	9310	31 200		1010	27640	73.8	51.
56 57	30	75 75	400 400	10	/	329 329		9090		21290	94.3			3.0	
57 58	30 30	75	400	20	512 512	329 329	9030	9290 8720	9520 9060	21490	94.6		27640 27720	63.4	53.
59	30	75		30	532					20930	94.7			61.6	
59 60	30	75	400 400	40	532	343	8860 9240	9120	9460 9870	21840 22740	94.7	1680	27720 27720	61.5 61.4	54.
-	~		300	1 "	<i>"</i> "	/50	7.40	, ,,,,,	10/0	.2/40	(7.1	.300	21120	**	,
61	30	100	300	5	518	331	9330	9600	9920	21860	94.6		25560	93.9	63.
62	30	100	300	10	518	331	9650	9920	10240	22180	95.0		25560	81.9	63.
63	30	100	300	20	518	331	9030	9280	0136	21550	95.1	1550	25560	78.5	63.
64	30	106	300	30	539	344	9350	9620	9960	22400	95.1		25560	78.3	63.
65	30	100	300	40	560	357	9680	9960	10310	23260	95.1	1550	25560	78.2	63.

TABLE 23
PHASE II DESIGN SUMMARY

Electrical	Min. Weight	Min. Volume
65	65	65
60	60	60
60	60	60
116	33	33
	65 60 60	65 65 60 60 60 60

APPENDIX A SELECTED ARTIST CONCEPTS AND SCHEMATICS

This appendix contains artist concepts and schematics for a minimum weight and a minimum volume design point for each of the four subsystems as selected by the Air Force. Each design has been based on intermittent operation with a maximum burst duration of two minutes.

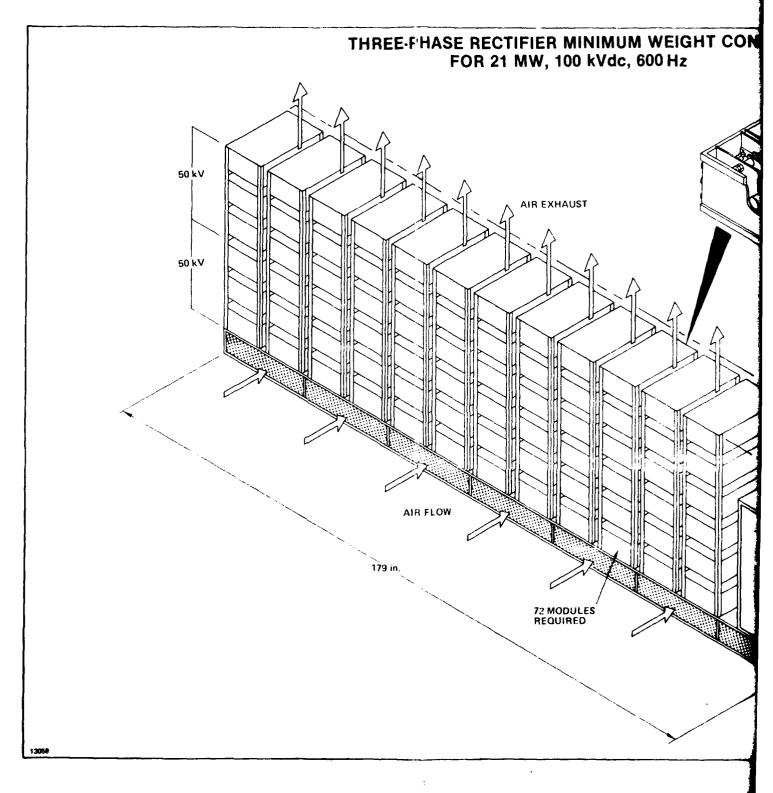


Figure 32 - Three-Phase

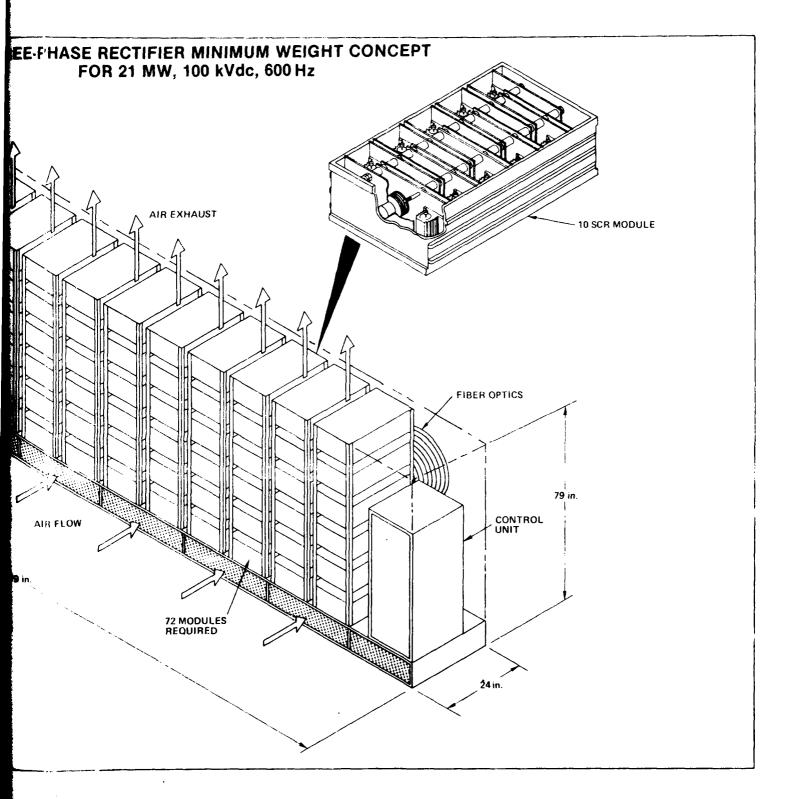


Figure 32 - Three-Phase Rectifier Minimum Weight Concept for 21 MW, 100 kVdc, 600 Hz

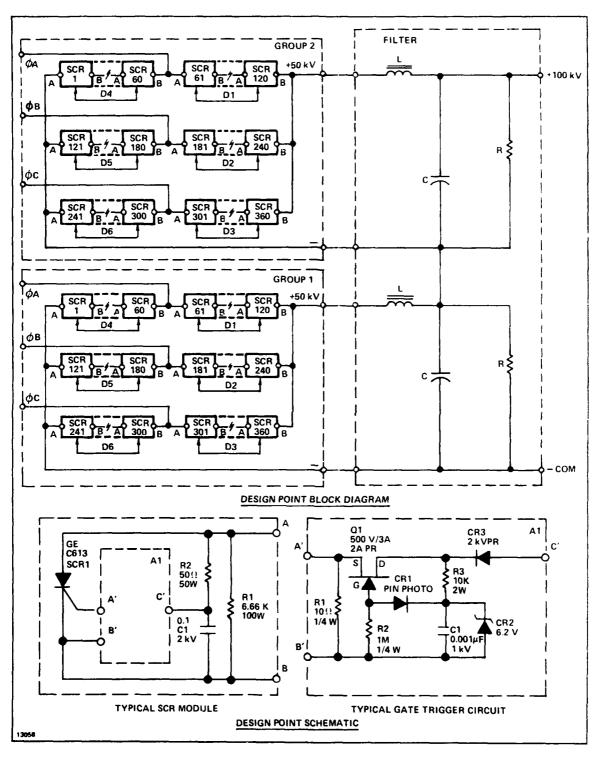


Figure 33 - Three-Phase Rectifier Schematic for 21 MW, 100 kVdc, 600 Hz

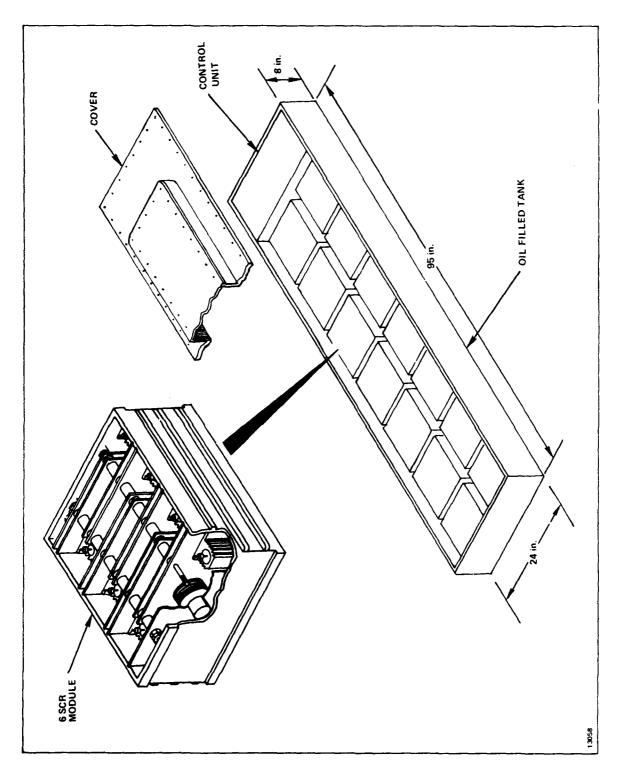
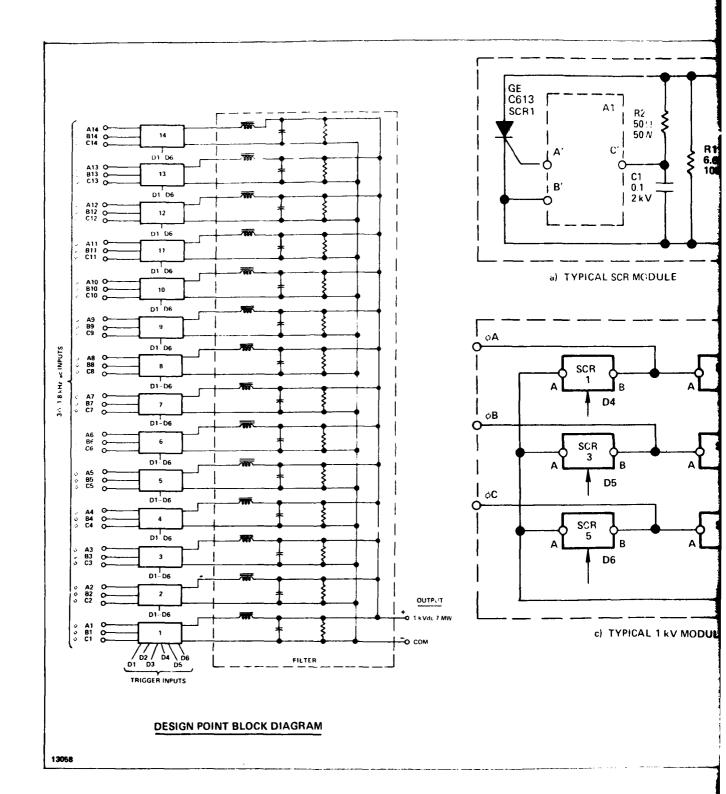


Figure 34 - Three-Phase Rectifier Minimum Volume Concept for 7 MW, 1 kVdc, 1.8 kHz



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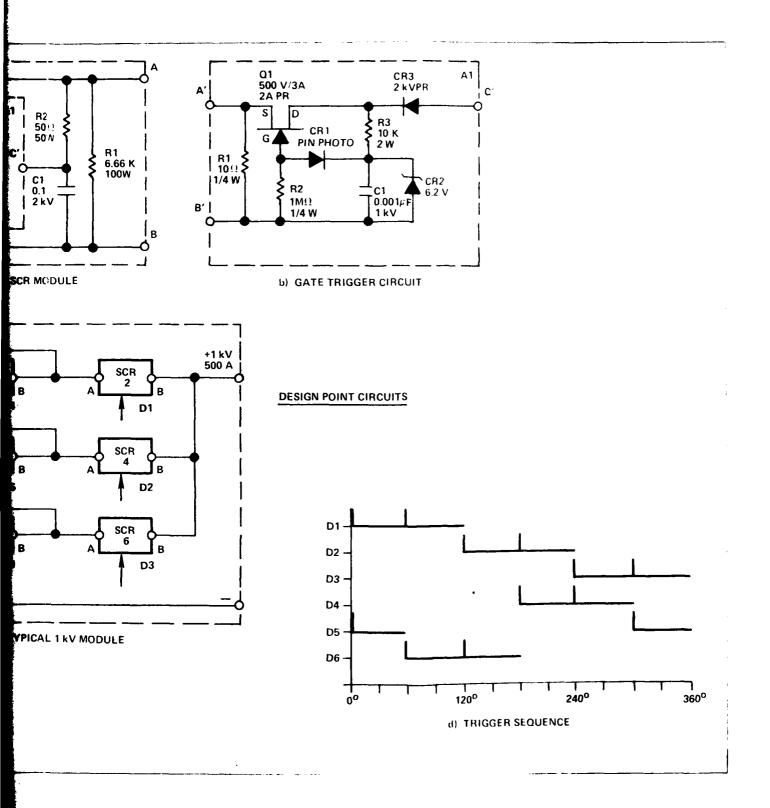
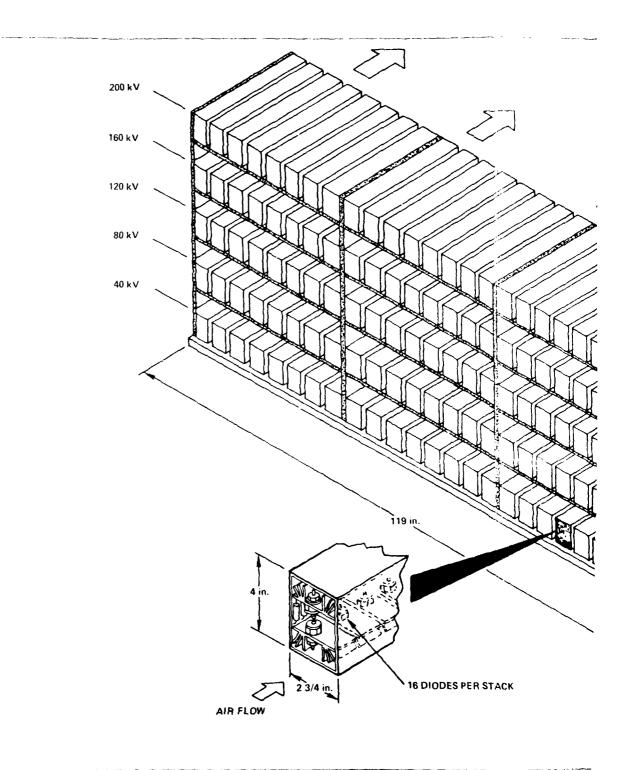


Figure 35 - Three-Phase Rectifier Schematic for 7 MW, 1 kVdc, 1.8 kHz



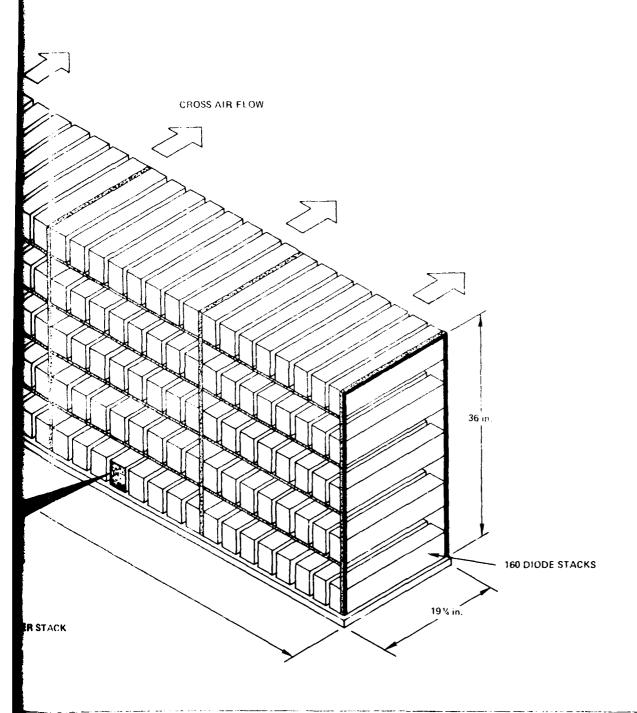
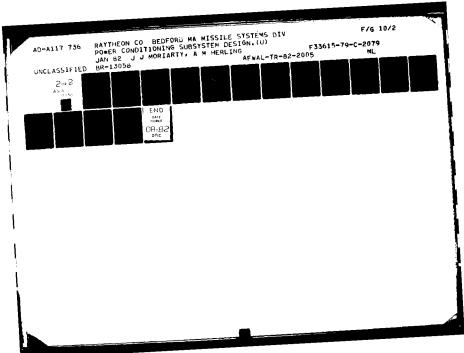
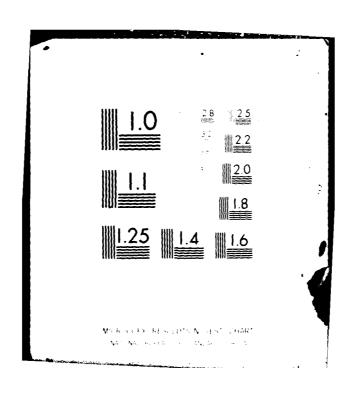


Figure 36 - Inverter-Fed Rectifier Minimum Weight Concept for 7 MW, 200 kVdc, 10 kHz





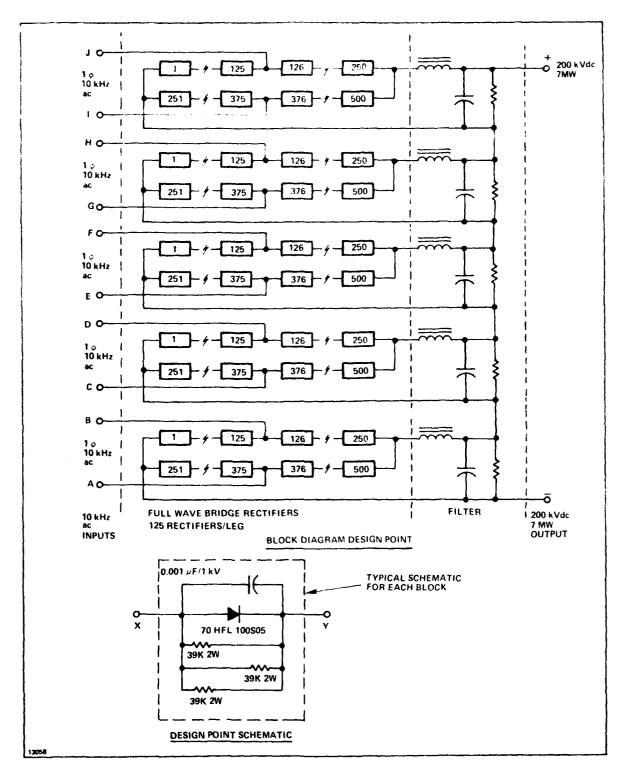
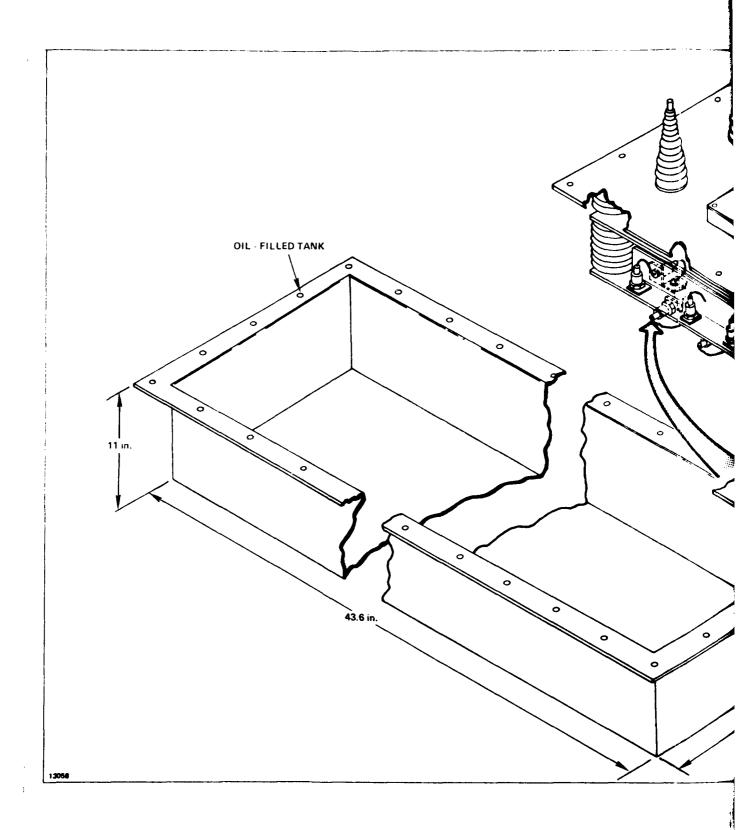


Figure 37 - Inverter-Fed Rectifier Schematic for 7 MW, 200 kVdc, 10 kHz



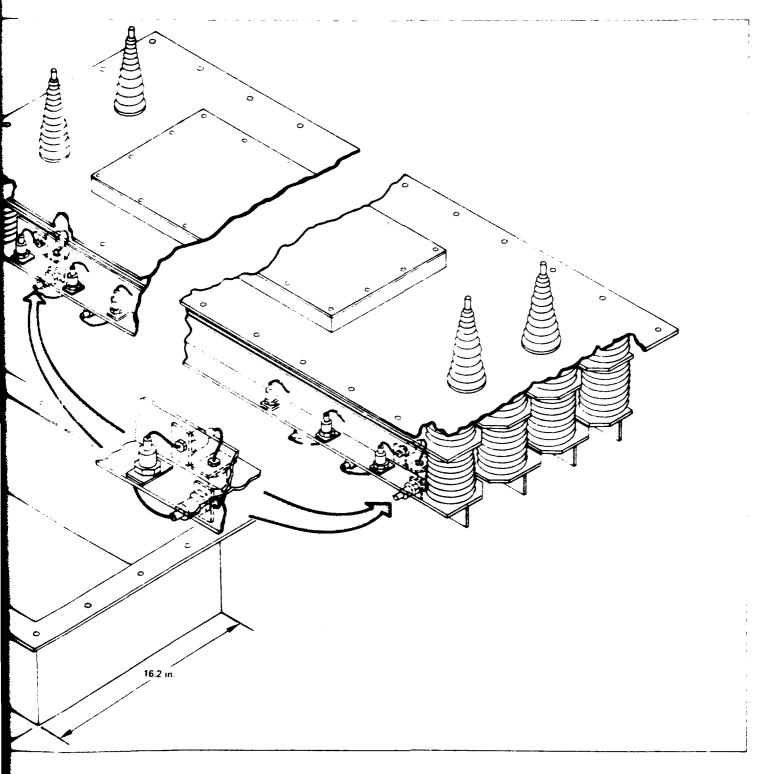


Figure 38 - Inverter-Fed Rectifier Minimum Volume Concept for 0.5 MW, 80 kVdc, 20 kHz

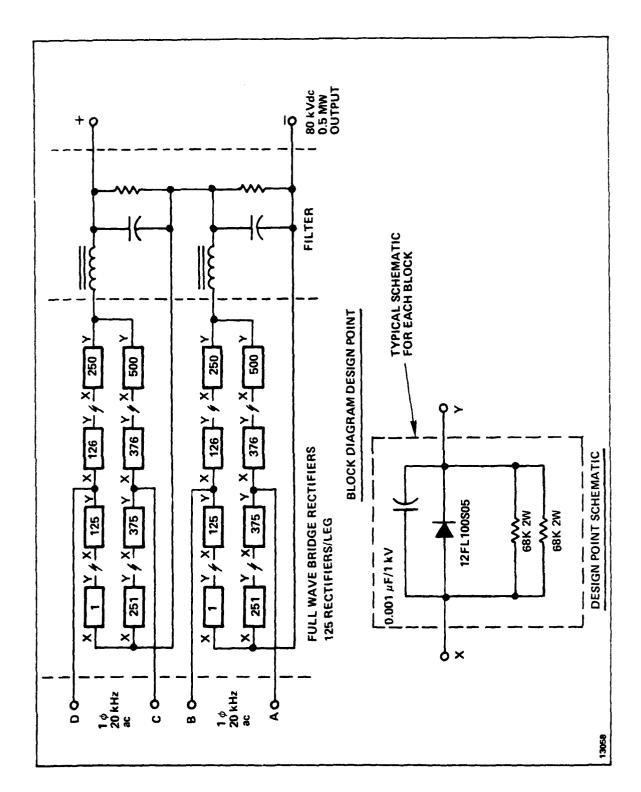


Figure 39 - Inverter-Fed Rectifier Schematic for 0.5 MW, 80 kVdc, 20 kHz

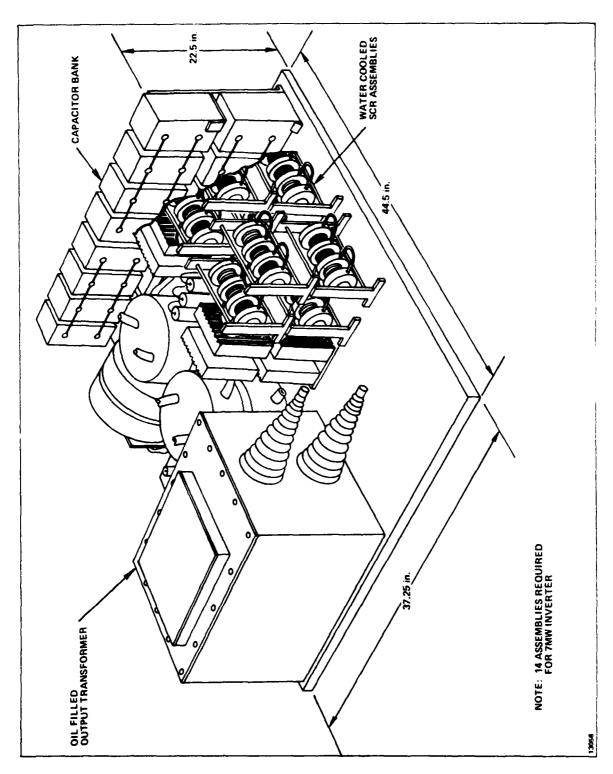


Figure 40 - Inverter Minimum Weight Concept for 7 MW, 1 kVdc in, 200 kVdc out, 10 kHz

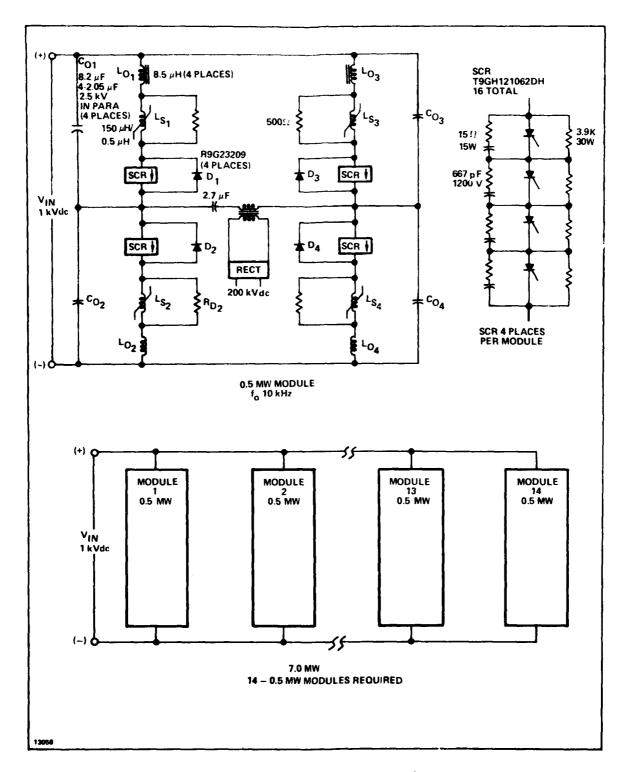
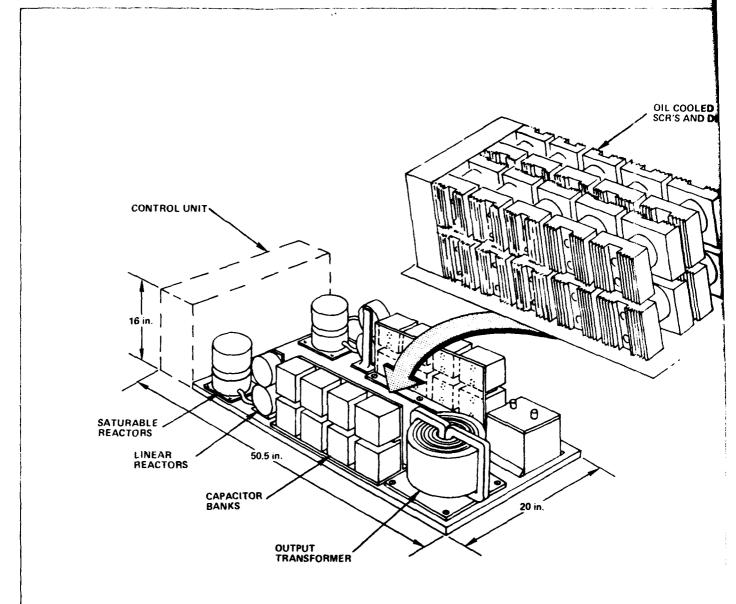


Figure 41 - Inverter Schematic for 7 MW, 1 kVdc in, 200 kVdc out, 10 kHz

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OIL INSULATED INVERTER ASSEMBLY

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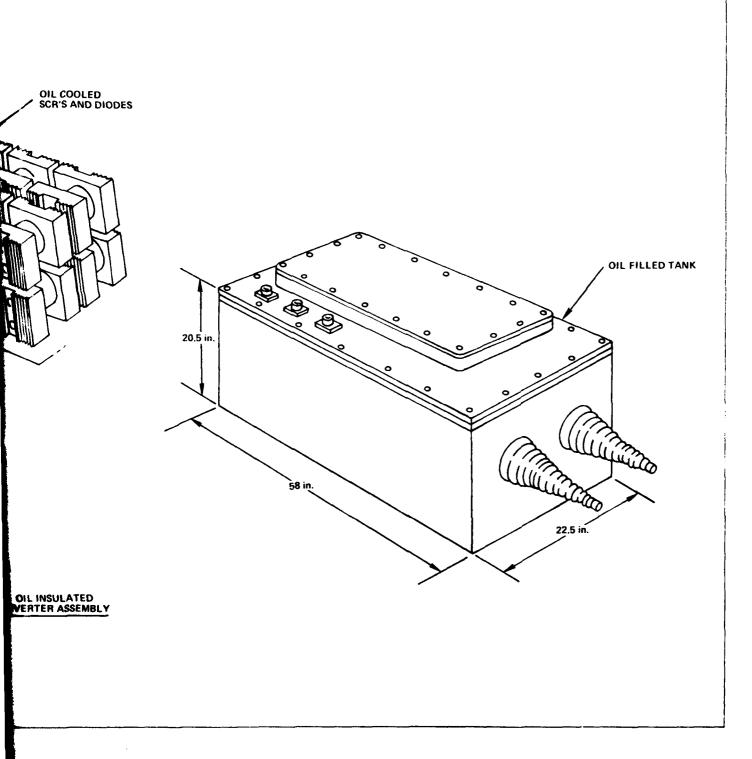


Figure 42 - Inverter Minimum Volume Concept for 0.5 MW, 1 kVdc in, 120 kVdc out, 15 kHz

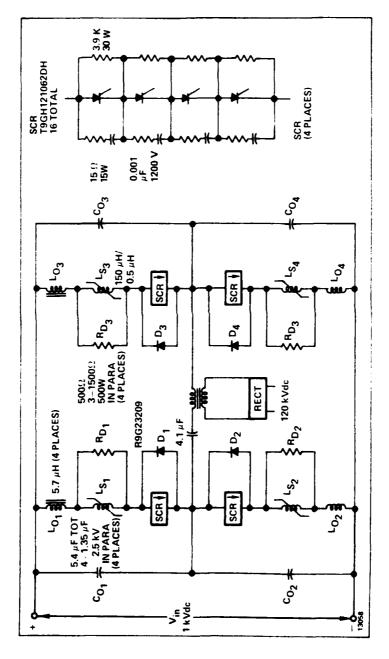


Figure 43 - Inverter Schematic for 0.5 MW, 1 kVdc in, 120 kVdc out, 15 kHz

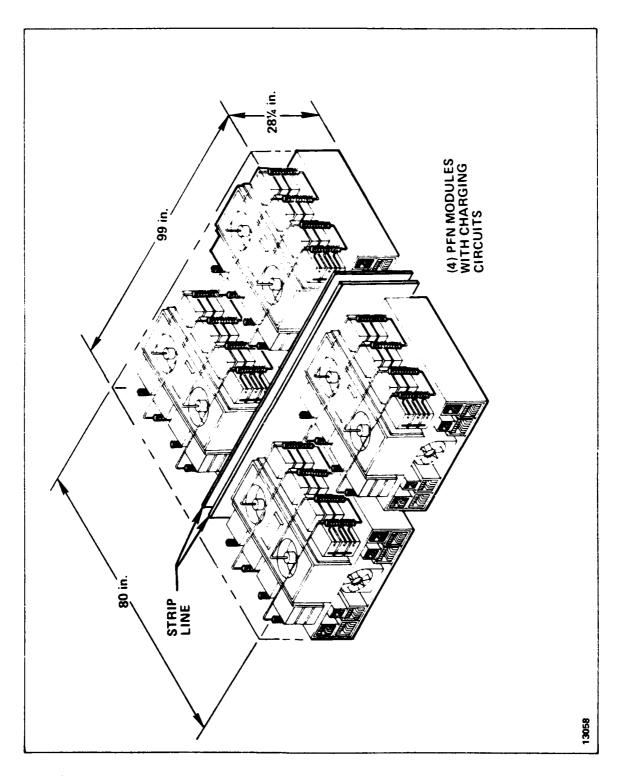
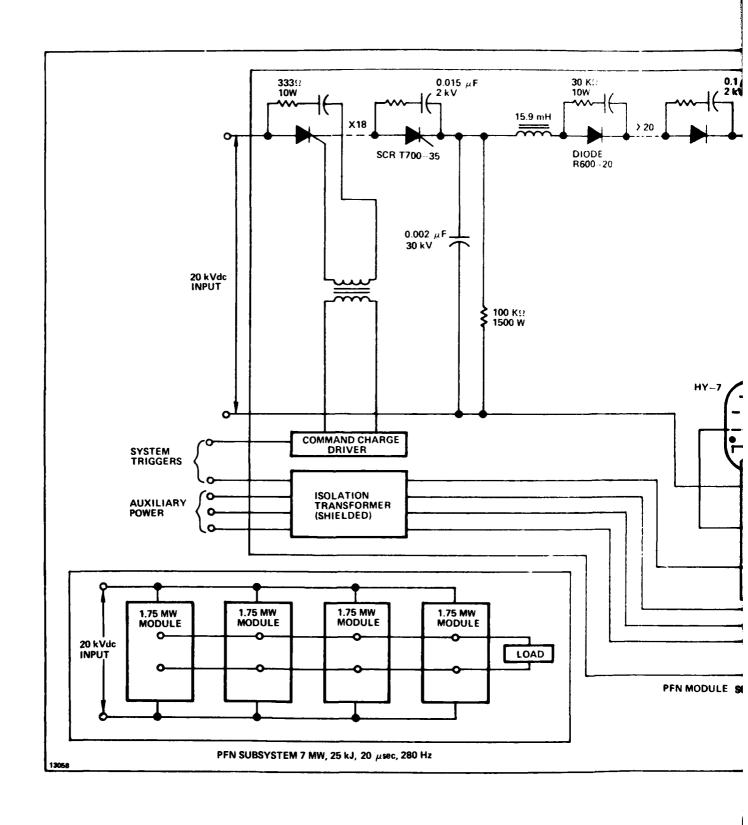


Figure 44 - PFN Minimum Weight Concept for 7 MW, 25 kJ, 20 μ sec, 280 Hz 90



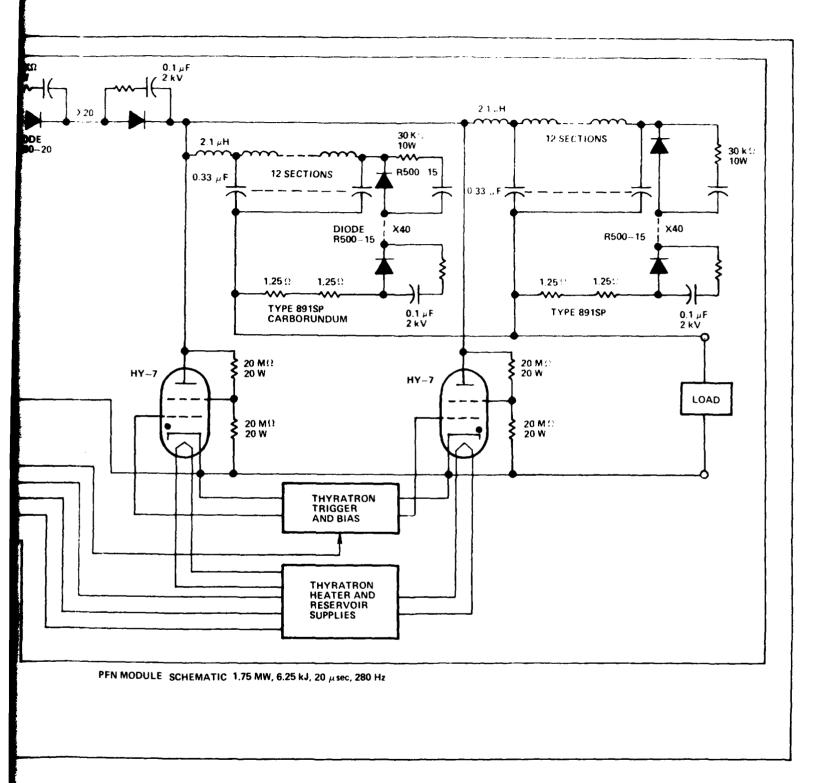
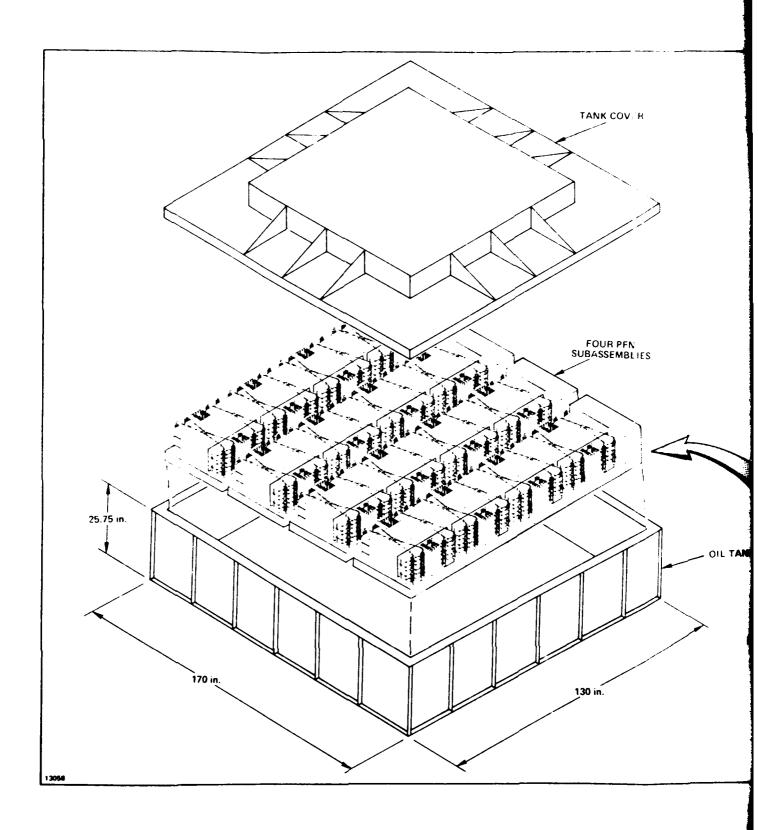


Figure 45 - PFN Schematic for 7 MW, 25 kJ, 20 μ sec, 280 Hz 91

C



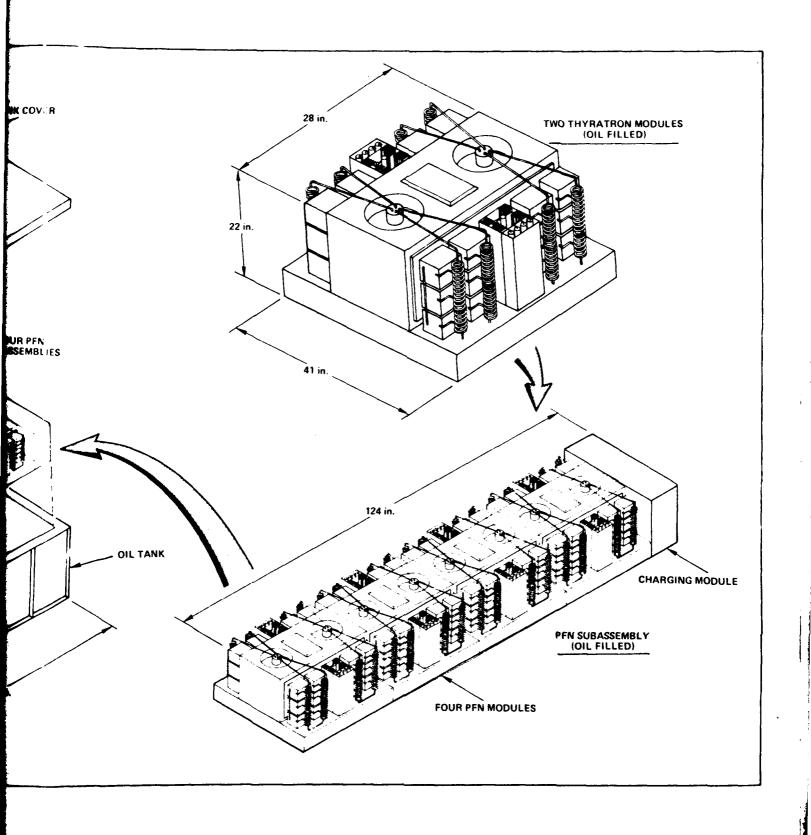


Figure 46 - PFN Minimum Volume Concept for 30 MW, 75 kJ, 5 μ sec, 400 Hz



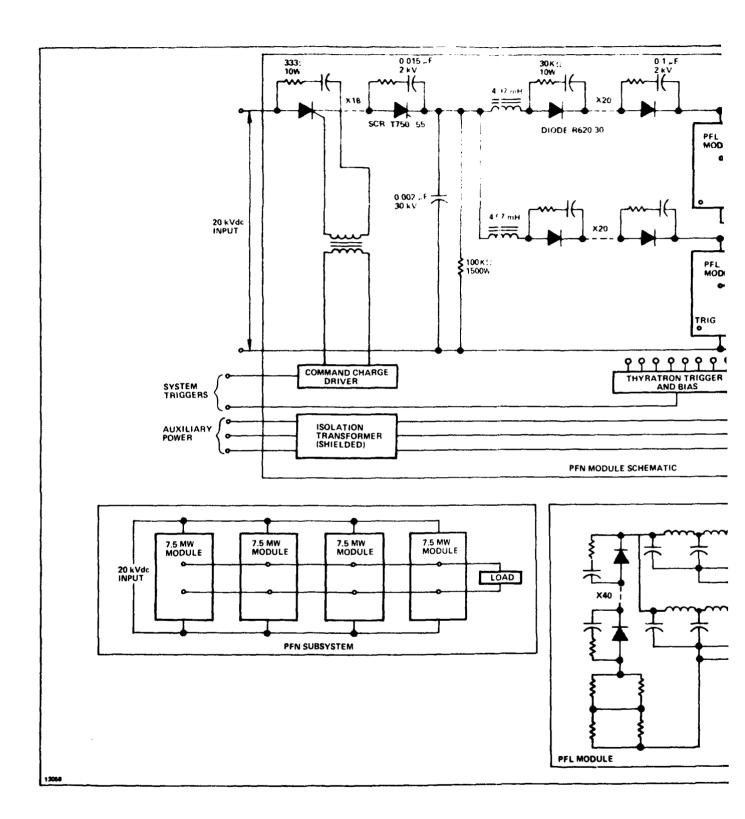


Figure 47 -

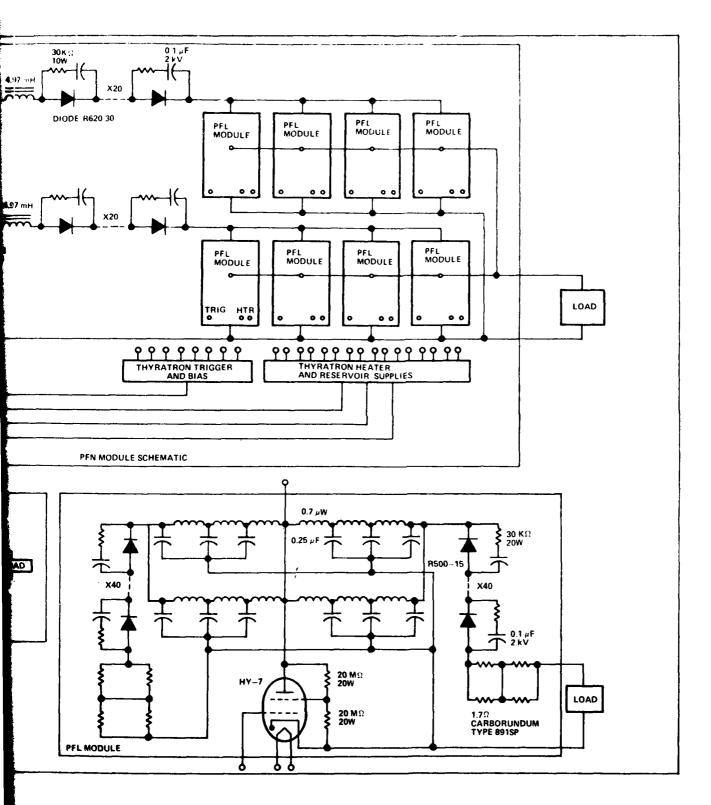


Figure 47 - PFN Schematic for 30 MW, 75 kJ, 5 $\mu\,sec,\,400~Hz$

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